Parallel VLSI CAD Algorithms

Lecture 1 Introduction
Zhuo Feng
Prof. Zhuo Feng
► Office: EERC 513
► Phone: 487-3116
► Email: zhuofeng@mtu.edu

Class Website
► http://www.ece.mtu.edu/~zhuofeng/EE5900Spring2012.html
► Check the class website for lecture materials, assignments, and announcements

Schedule
► TR 9:35am-10:50am EERC 218
► Office hours: TR 4:30pm – 5:30pm or by appointments
Textbook


References


Topics (tentative)

- Introduction
- Brief review of matrix theory, linear algebra and numerical methods
- Basic circuit analysis methods (Part 1, Part 2)
- IC interconnect modeling methods
- Model order reduction techniques (AWE, PRIMA)
- RF circuit simulation methods
- Introduction to emerging heterogeneous parallel computing platforms
- Parallel GPU-based simulation methods for power delivery networks.
- Full-chip thermal analysis on GPUs
- Parallel 3D capacitance extraction on GPU
**Project**

- This is a project/research oriented course.
- Research explorations are strongly encouraged.
- Students are expected to read research papers assigned before lectures and actively participate in class discussions.

**Grading**

- Assignment (course projects): 70%
- Exams: 30%

**No plagiarism!**
A plethora of VLSI CAD problems

Devices, interconnects, circuits, systems, signal, power, analog, digital ….
Where are we in the design flow?

- Specifications
  - System-level Design
  - RTL-level Design
  - Gate-level Design
  - Transistor/Circuit Level
  - Layout
  - Final Verification

Top-down Design

Bottom-up Verification

Electrical & Thermal Properties, Delays, Waveforms, Parasitics Effects, Coupling Noise ...
Why circuit analysis?

Performance verification

- A critical step for evaluating expected performance prior to manufacturing

- Simulation is always cheaper and more efficient than actually making the chip

- True more than ever for today’s high manufacturing costs
Why circuit simulation (cont’d) ?

► Design optimization/synthesis

▼ Need to evaluate circuit performances many times in an optimization loop before meeting all the specs

▼ Can only be practically achieved via simulation (models)

![Diagram](image)

Circuit Optimizer

Meet all specs?

Convergence

No

Yes

Update design parameters

Simulation Engine

Performance Evaluation

Z. Feng  MTU EE5900 Spring 2012
Why models?

- Models are integral parts of system simulation and/or optimization

- Abstract Executable Models
  - High
  - Low

- Cycle Accurate Models
  - High
  - Low

- VHDL/Verilog Models
  - Speed

- Interconnect Gate Models
  - Low
  - High

- Device Models
Assessment of simulators

- Accuracy
- Robustness/Applicability
- Runtime
- Memory

Z. Feng  MTU EE5900 Spring 2012
Selected Topics

- Classical circuit simulation methods (SPICE)
  - LU factorization, Newton’s method
  - (Modified) nodal formulation (MNA)
  - Nonlinear DC analysis
  - AC analysis
  - Linear/nonlinear transient analyses
  - SPICE device models
Many problems are modeled by some form of coupled (nonlinear) first-order differential equations.

For circuit problems this is usually done using MNA formulation.
■ Write KCL (Kirchhoff’s Current Law) at node 1:

\[ C \frac{d(v_1 - v_3)}{dt} + \frac{(v_1 - v_4)}{R} - f(v_2 - v_1) = 0 \]

■ If we do this for all N nodes:

\[ F(\vec{x}(t),\vec{x}(t),\vec{u}(t)) = 0 \quad \vec{x}(0) = \vec{X} \]

\[ \vec{x}(t) = \text{N dimensional vector of unknown node voltages} \]
\[ \vec{u}(t) = \text{vector of independent sources} \]
\[ F = \text{nonlinear operator} \]
How can we solve this set of nonlinear differential equations?

\[ F(\ddot{x}(t), \dot{x}(t), u(t)) = 0 \quad \ddot{x}(0) = \dddot{X} \]

- Closed-form formula/hand analysis easily becomes infeasible
- Need to develop computer programs (circuit simulators) to solve for the solution numerically
Selected Topics

► Elmore delay
► Timing simulation
► Intend to evaluate the circuit timing quickly
  ▼ Crucial for large VLSI circuit synthesis/optimization
  ▼ Provide delay estimation or waveform approximation using easy-to-compute metrics or (approximated) timing simulation

\[ T_{D4} = R1(C1 + C2 + C3 + C4) + R2(C2 + C3 + C4) + R4C4 \]
Selected Topics

- Model order reduction

- Key drivers for achieving feasible simulation
  - IC interconnect analysis
  - Whole system verification
  - Design space exploration
Selected topics

► Parallel CAD

Courtesy Intel

Courtesy AMD

Courtesy TI

Original Problem / GMRES Solver

Sub-problem / GMRES solver

Sub-problem / GMRES solver

Sub-problem / GMRES solver

Z. Feng  MTU EE5900 Spring 2012
GPU Computing for CAD

- Dedicated for graphics rendering

Video Out

GPU is connected to MCH via 16x PCI-Express
Reading assignments

- Textbook. Chapters 1 and 2

History of SPICE

- CANCER at UCB: Computer Analysis of Nonlinear Circuits Excluding Radiation

- Government project SCEPTRE: System for Circuit Evaluation and Prediction of Transient Radiation Effects

- CANCER evolved to SPICE: Simulation Program with Integrated Circuit Emphasis

- SPICE became the industry standard
SPICE overview

- N equations in terms of N unknown Node voltages
- More generally using modified nodal analysis
Time Domain Equations at node 1:

\[ C \frac{d (v_1 - v_3)}{dt} + \frac{(v_1 - v_4)}{R} - G(v_2 - v_1) = 0 \]

▶ If we do this for all N nodes:

\[ F(\vec{x}(t), \vec{x}(t), \vec{u}(t)) = 0 \quad \vec{x}(0) = \vec{X} \]

\[ \vec{x}(t) = \text{N dimensional vector of unknown node voltages} \]

\[ \vec{u}(t) = \text{vector of independent sources} \]

\[ F = \text{nonlinear operator} \]
■ Closed form solution is not possible for arbitrary order of differential equations

■ We must approximate the solution of:

\[ F(\ddot{x}(t), \dot{x}(t), u(t)) = 0 \quad \ddot{x}(0) = \ddot{X} \]

■ This is facilitated in SPICE via numerical solutions
Basic circuit analyses

► (Nonlinear) DC analysis
  ▼ Finds the DC operating point of the circuit
  ▼ Solves a set of nonlinear algebraic eqns

► AC analysis
  ▼ Performs frequency-domain small-signal analysis
  ▼ Require a preceding DC analysis
  ▼ Solves a set of complex linear eqns

► (Nonlinear) transient analysis
  ▼ Computes the time-domain circuit transient response
  ▼ Solves a set of nonlinear different eqns
  ▼ Converts to a set nonlinear algebraic of eqns using numerical integration
SPICE offers practical techniques to solve circuit problems in time & freq. domains

- Interface to device models
  - Transistors, diodes, nonlinear caps etc

- Sparse linear solver

- Nonlinear solver – Newton-Raphson method

- Numerical integration

- Convergence & time-step control
Circuit equations are usually formulated using

- Nodal analysis
  - N equations in N nodal voltages

- Modified analysis
  - Circuit unknowns are nodal voltages & some branch currents
  - Branch current variables are added to handle
    - Voltages sources
    - Inductors
    - Current controlled voltage source etc

Formulations can be done in both time and frequency
How do we set up a matrix problem given a list of linear(ized) circuit elements?

Similar to reading a netlist for a linear circuit:

<table>
<thead>
<tr>
<th>* Element Name</th>
<th>From</th>
<th>To</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_1$</td>
<td>0</td>
<td>1</td>
<td>1mA</td>
</tr>
<tr>
<td>$R_1$</td>
<td>1</td>
<td>0</td>
<td>10Ω</td>
</tr>
<tr>
<td>$R_2$</td>
<td>1</td>
<td>2</td>
<td>5Ω</td>
</tr>
<tr>
<td>$R_3$</td>
<td>2</td>
<td>0</td>
<td>100Ω</td>
</tr>
</tbody>
</table>
The nodal analysis matrix equations are easily constructed via KCL at each node:

\[ Y\bar{v} = \bar{J} \]
Naïve approach
  a) Write down the KCL eqn for each node
  b) Combine all of them to get N eqns in N node voltages

Intuitive for hand analysis

Computer programs use a more convenient “element” centric approach
  Element stamps
Instead of converting the netlist into a graph and writing KCL eqns, *stamp* in elements one at a time:

**Stamps: add to existing matrix entries**

\[
Y = \begin{bmatrix}
\frac{1}{R} & -\frac{1}{R} \\
-\frac{1}{R} & \frac{1}{R}
\end{bmatrix}
\]

- From row \(i\)
- To row \(j\)
- From col. \(i\)
- To col. \(j\)
RHS $\vec{j}$ of equations are stamped in a similar way:
Stamping our simple example one element at a time:

\[
\begin{align*}
I_1 & \quad 0 \quad 1 \quad 1 \text{mA} \\
R_1 & \quad 1 \quad 0 \quad 10 \ \Omega \\
R_2 & \quad 1 \quad 2 \quad 5 \ \Omega \\
R_3 & \quad 2 \quad 0 \quad 100 \ \Omega \\
\end{align*}
\]

\[
\begin{bmatrix}
G_1 + G_2 & -G_2 \\
-G_2 & G_2 + G_3
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix}
=
\begin{bmatrix}
I_1 \\
0
\end{bmatrix}
\]
We know that nonlinear elements are first converted to linear components, then stamped

\[ I_{EQ}, G_{EQ} \]
For 3 & 4 terminal elements we know that the linearized models have linear controlled sources.

We can stamp in MOSFETs in terms of a complete stamp, or in terms of simpler element stamps.
Voltage controlled current source

\[ i = g_m v_{kl} \]

\[ v_{kl} \]

\[ I = 0 \]

Voltmeter

Large value that does not fall on diagonal of Y!
- All other types of controlled sources include voltage sources

- Voltage sources are inherently incompatible with nodal analysis

- Grounded voltages sources are easily accommodated

\[
\begin{bmatrix}
1 & \cdots & \vdots & \vdots & \vdots \\
2 & v_1 & v_2 & \vdots & \vdots \\
\end{bmatrix} = \begin{bmatrix} 2 \end{bmatrix}
\]
But a voltage source in between nodes is more difficult.

Node voltages $k$ and $l$ are not independent.
We no longer have \( N \) independent node voltage variables

So we can potentially eliminate one equation and one variable

But the more popular solution is modified nodal analysis (MNA)

Create one extra variable and one extra equation
Extra variable: voltage source current

Allows us to write KCL at nodes $k$ and $l$

Extra equation

$$v_k - v_l = V$$

Advantage: now have an easy way of printing current results - - ammeter
Voltage source stamp:

\[
\begin{array}{ccc}
\text{row } k & \begin{bmatrix} 1 \\ -1 \end{bmatrix} & = \\
\text{row } \ell & \begin{bmatrix} 1 \\ -1 \end{bmatrix} & \begin{bmatrix} i \end{bmatrix} \\
\text{row } N+1 & \begin{bmatrix} 1 & -1 & 0 \end{bmatrix} & \begin{bmatrix} V \end{bmatrix}
\end{array}
\]
Current-controlled current source (e.g. BJT) has to stamp in an ammeter and a controlled current source

\[ i_2 = \alpha i_1 \]
In general, we would not blindly build the matrix from an input netlist and then attempt to solve it.

Various illegal ckt{s are possible:

**Cutsets of current sources**

![Diagram of a circuit with a current source and a cutset](image-url)
Loops of voltage sources

Dangling nodes
Once we efficiently formulate MNA equations, an efficient solution to $Y\bar{V} = J$ is even more important.

For large circuits the matrix is really sparse.
- Number of entries in $Y$ is a function of number of elements connected to the corresponding node.

Inverting a sparse matrix is never a good idea since the inverse is not sparse!

Instead direct solution methods employ Gaussian Elimination or LU factorization.
Reading assignment:
  ► Textbook, sections 3.1-3.4, 7.1-7.5

We need to solve a linear matrix problem for the simple DC circuit

Linear system solutions are also basic routines for many other analyses
  ► Transient analysis, nonlinear iterations etc

Sounds quite easy but can become nontrivial for large analysis problems
  ► $O(n^3)$ – general dense matrices
  ► $O(n^{1.1} \sim n^{1.5})$ -- sparse circuit problems
  ► $O(n^{1.5})$ – 2D mesh  $O(n^2)$ – 3D mesh