Scalable Vectorless Power Grid Current Integrity Verification
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(I) Motivation
- Shrinking feature sizes and dramatically increased power densities may result in greater current densities in modern PDN designs.
- Assessing worse-case electromigration (EM) effects will become a routine job for power grid designers.
- Power grid current integrity verification can be as important/difficult as voltage integrity verifications.

(II) Background
- Linear programming (LP) formula for maximizing voltage difference across a specific wire:
  \[
  \text{Maximize: } V_i - V_j = \epsilon_i - \epsilon_j \ E^T \ \text{for}\ \ i = 1, \ldots, n , \text{where}\ \ E = G^T; G_i = b_k \text{ and } \epsilon_i = [0, \ldots, 1, \ldots, 0]
  \]
  s.t. the \text{local and global constraints:} \ E^T b_i \leq b_k \leq E^T b_j.
- Multi-level current integrity verification framework:
  - Create a hierarchy of current verification problems ordered from finest to coarsest levels.
  - Successively/ incrementally tackle the coarsest to the finest level verification problems.

(III) Key Components in Power Grid Current Integrity Verification
- Extra voltage difference contributed by the currents outside the critical region:

<table>
<thead>
<tr>
<th>Current constraints for coarser to coarsest</th>
<th>[ \text{Fine Grid} ]</th>
<th>[ \text{Coarse Grid} ]</th>
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<tbody>
<tr>
<td>[ -0.01 ]</td>
<td>[ -0.008 ]</td>
<td>[ -0.006 ]</td>
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<td>[ -0.004 ]</td>
<td>[ -0.002 ]</td>
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- Coarse grid verification solution vectors are mapped onto finer grids:
  - Evenly distribute coarse grid solution (current vectors) onto the finer grids.

- Are the projected results good enough?
  - Not always true: inter-grid operations (mapping) may introduce some errors.
  - A local solution refinement step is proposed to significantly improve the solution quality.

(IV) EM-Aware Flip-Chip Power Grid Reduction
- Stage One: Geometric Template Construction
  1. Construct the coarse grid template based on the original power grid layout;
  2. Stamp individual circuit components, such as circuit nodes, resistors, capacitors, and current excitation sources, onto the reduced template grid;
  3. Merge the nodes, wires, capacitors and current sources of the original grid that fall onto the same nodes, wires, capacitors and current sources of the template grid;

- Stage Two: Iterative Template Grid Correction
  1. Perform iterative block grid corrections to match electrical behaviours;
  2. If the reduction errors are not acceptable, correct the coarse grid by introducing more nodes into the reduced grids, and repeat the above steps 1-5;
  3. Finalize the PG reduction and output the reduced power grid netlist.

(V) Scalable Current Integrity Verification with Critical Regions
- Adjoint sensitivity analysis is used to find critical regions:
  - If a voltage difference w.r.t a specific current source is smaller than the threshold, it will fall into the \text{global or local critical regions}.
  - Global critical regions are defined for the coarsest level grid.
  - Local critical regions are defined for the coarsest to finest level grids.

- Extra voltage difference contributed by the currents outside the critical region:
  \[ V_i - V_j = \epsilon_i - \epsilon_j \ E^T \ \text{for}\ \ i = 1, \ldots, n , \text{where}\ \ E = G^T; G_i = b_k \text{ and } \epsilon_i = [0, \ldots, 1, \ldots, 0] \]
  s.t. the \[ -0.01 \leq b_i \leq 0 \leq b_j \text{.} \text{Err.} \]

- Upper/lower bounds for worst case voltage difference:
  \[ V_{\text{worst}} \leq V_{\text{worst}} + V_{\text{worst}} + \epsilon_i - \epsilon_j \ E^T \ \text{for}\ \ i = 1, \ldots, n , \text{where}\ \ E = G^T; G_i = b_k \text{ and } \epsilon_i = [0, \ldots, 1, \ldots, 0] \]
  \[ V_{\text{worst}} \leq V_{\text{worst}} + V_{\text{worst}} + \epsilon_i - \epsilon_j \ E^T \ \text{for}\ \ i = 1, \ldots, n , \text{where}\ \ E = G^T; G_i = b_k \text{ and } \epsilon_i = [0, \ldots, 1, \ldots, 0] \]

- Tradeoffs between solution quality and verification cost

(VI) Experimental Results
- Test Case Setup
  - Seven flip-chip power grids of various sizes
  - Generated according to typical wire resistances & current source distributions of industrial designs
  - LP_Solve is applied to solve the linear programs in the current verification problem

- DC and TR Analysis Results for EM-aware PG reductions
  - Pad Error w/o correction
  - Pad Error w/ correction

- Critical Region for Current Integrity Verification

- Results of the multilevel PG current integrity verification

- The logarithmic scale sensitivity map for the voltage difference across a specific wire located at (65, 76)