Scalable Vectorless Power Grid Current Integrity Verification

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(I) Motivation

- Shrinking feature sizes and dramatically increased power densities may result in greater current densities in modern PDN designs.
- Assessing worse-case electromigration (EM) effects will become a routine job for power grid designers.
- Power grid current integrity verification can be as important/difficult as voltage integrity verifications.

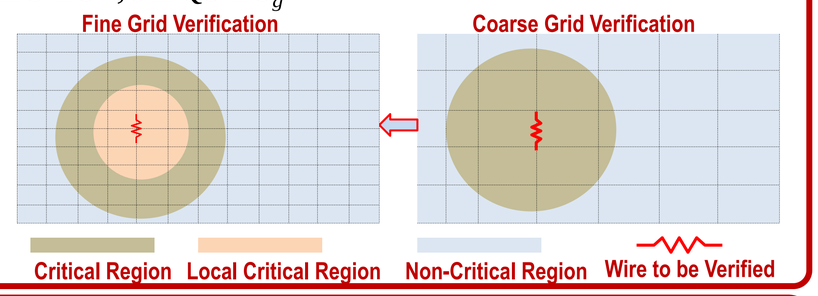
(II) Background

- **Linear programming (LP) formula for maximizing voltage difference across a specific wire :**

  Maximize: $v_i - v_j = e_i^T - e_j^T \; E^{-1} b$ **for** $i = 1, \cdots, n$ **,where** $E = G^{-1}$, $G \cdot v = b$ **and** $e_i = [0, \cdots, 1, \cdots, 0]$

  S. t. the local and global current constraints: $b^L \le b \le b^U, 0 \le Qb \le b_g$

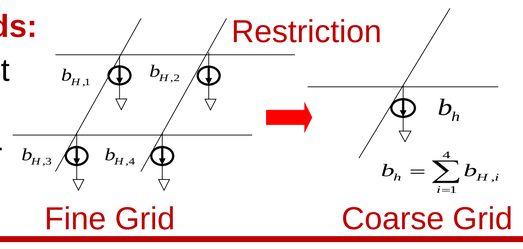
- **Multilevel current integrity verification framework:**
  - Create a hierarchy of current verification problems ordered from finest to coarsest levels
  - Successively/incrementally tackle the coarsest to the finest level verification problems



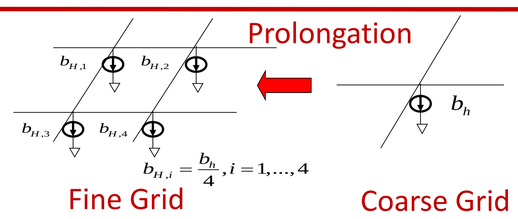
(III) Key Components in Power Grid Current Integrity Verification

- **Key components in multilevel power grid current verification:**
  - **1. EM-aware power grid reduction for creating replicas of the original problem;**
  - **2. Local & global current constraints mapping from fine grid to coarse grid;**
  - **3. Verification solution vector mapping from coarse grid to fine grid;**
  - **4. LP solver will be adopted for verification of each level problem;**
  - **5. Solution refinement is critical for improving the verification accuracy.**

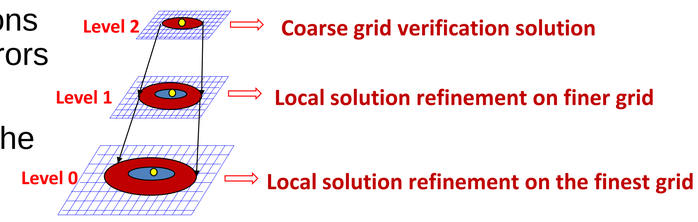
- **Current constraints for coarser to coarsest grids:**
  - Simple location-based (functional blocks) current collection scheme can be applied
  - Satisfactory performance has been observed for flip-chip power grid design verifications



- **Coarse grid verification solution vectors are mapped onto finer grids**
  - Evenly distribute coarse grid solution (current vectors) onto the fine grids

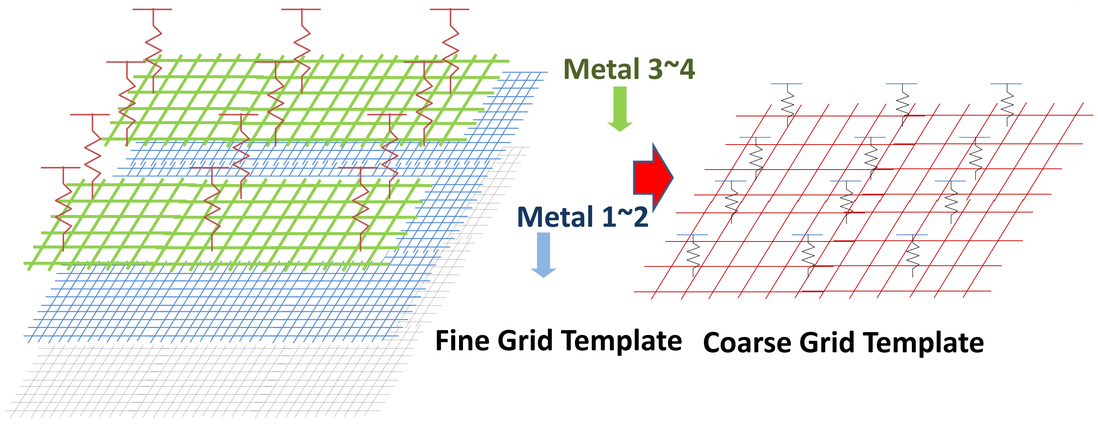


- **Are the projected results good enough?**
  - Not always true: inter-grid operations (mapping) may introduce some errors
  - A local solution refinement step is proposed to significantly improve the solution quality

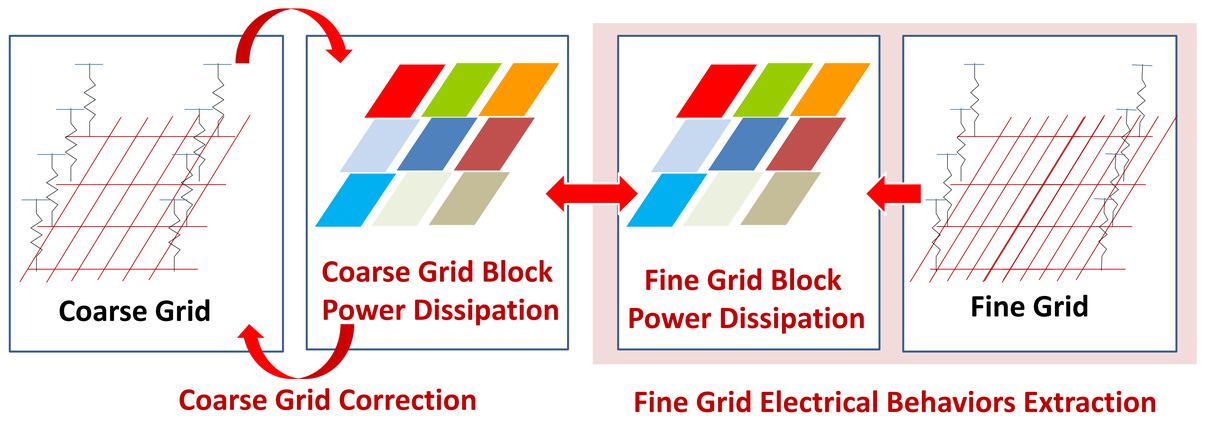


(IV) EM-Aware Flip-Chip Power Grid Reduction

- **Stage One: Geometric Template Construction**
  - **1.** Construct the coarse grid template based on the original power grid layout;
  - **2.** Stamp individual circuit components, such as circuit nodes, resistors, capacitors, and current excitation sources, onto the reduced template grid;
  - **3.** Merge the nodes, wires, capacitors and current sources of the original grid that fall onto the same nodes, wires, capacitors and current sources of the template grid;

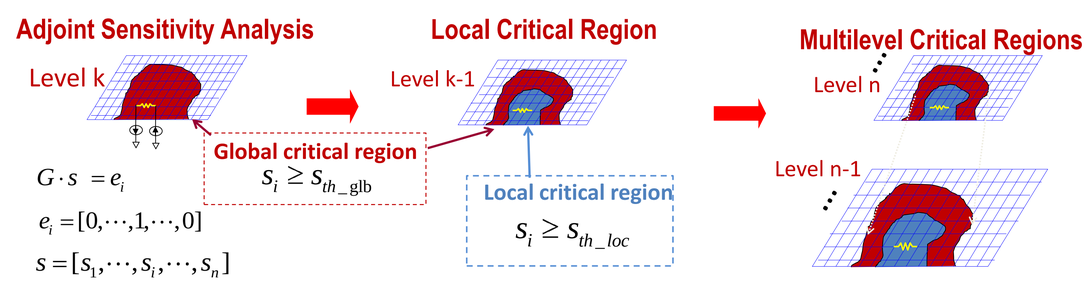


- **Stage Two: Iterative Template Grid Correction**
  - **4.** Perform iterative block grid corrections to match electrical behaviours;
  - **5.** If the reduction errors are not acceptable, correct the coarse grid by introducing more nodes into the reduced grids, and repeat the above steps 1-5;
  - **6.** Finalize the PG reduction and output the reduced power grid netlist.



(V) Scalable Current Integrity Verification with Critical Regions

- **Adjoint sensitivity analysis is used to find critical regions**
  - If a voltage difference *w.r.t* a specific current source is smaller than the threshold s_{th}, it will fall into the *global or local critical regions*
    - Global critical regions are defined for the coarsest level grid
    - Local critical regions are defined for the coarser to finest level grids



- **Extra voltage difference contributed by the currents outside the critical region:**

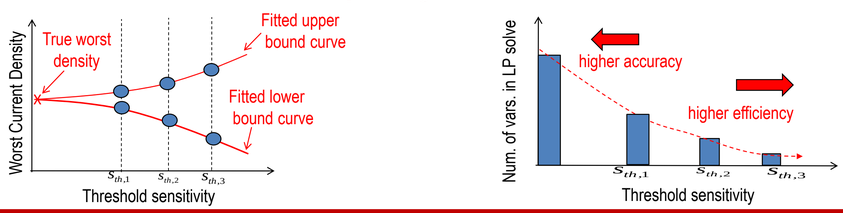
$$v_e = \max_{\forall b_i \notin C_{\text{glb}}} \left(\sum_{i=1}^{n} s_i b_i \right) \le \max_{\forall b_i \notin C_{\text{glb}}} \left(\sum_{i=1}^{n} s_{th} b_i \right) = s_{th} \left| b - b_p \right|_1$$

, where b_p is a current vector including all the currents within C_{glb}

- **Upper/lower bounds for worst case voltage difference:** $\bar{v}_{wst} \le v^*_{wst} \le v_{wst}$

$$\bar{v}_{wst} \le v^*_{wst} \le \bar{v}_{wst} + v_e \le \bar{v}_{wst} + s_{th} \left| b - b_p \right|_1 = v_{wst}$$

- **Tradeoffs between solution quality and verification cost**



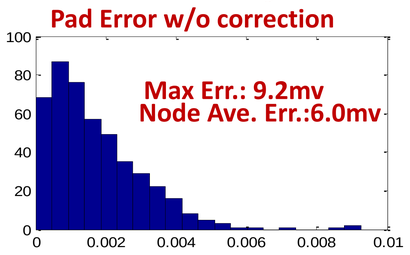
(VI) Experimental Results

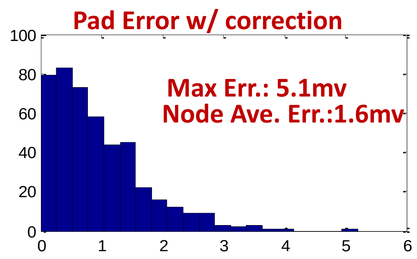
Test case setup

- Seven flip-chip power grids of various sizes
- Generated according to typical wire resistances & current source distributions of industrial designs
- LP_Solve is applied to solve the linear programs in the current verification problem

Circuit	# of Nodes	# of Cur.	# of Lev.
CKT1	44K	10K	2
CKT2	67K	18K	2
CKT3	131K	32K	2
CKT4	168K	39K	2
CKT5	256K	78K	2
CKT6	511K	151K	3
CKT7	1.02M	300K	2

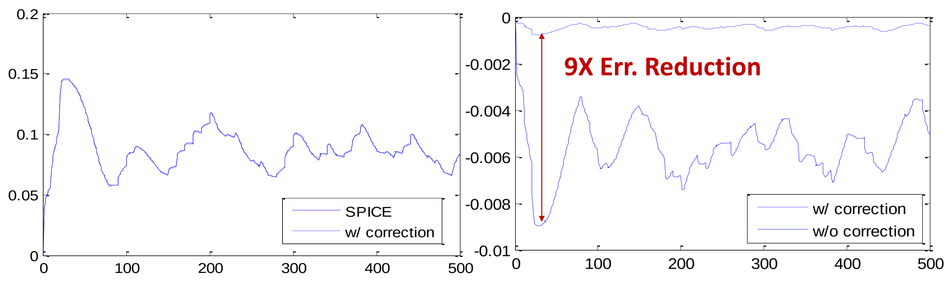
DC and TR Analysis Results for EM-aware PG reductions



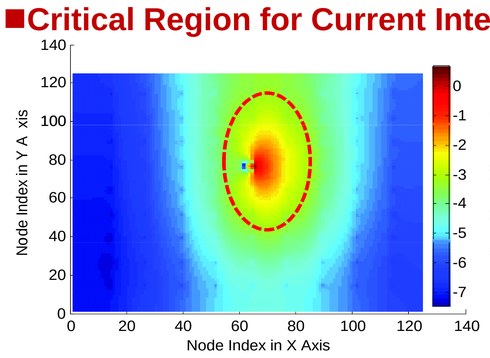


Time Domain Waveforms (V)

Time Domain Waveform Errors (V)



Critical Region for Current Integrity Verification



The logarithmic scale sensitivity map for the voltage difference across a specific wire located at (65, 76)

Results of the multilevel PG current integrity verification

	PG Des. Specs.			$\varepsilon_{\text{glb}} = 5e-3, \beta = 2$			$\varepsilon_{\text{glb}} = 10e-3, \beta = 2$				$\varepsilon_{\text{glb}} = 20e-3, \beta = 1.5$			
CKT	N_{nodes}	N_{cur}	N_{lev}	T_{glb}	T_{ref}	T_{tot}	T_{glb}	T_{ref}	T_{tot}	$Err.$	T_{glb}	T_{ref}	T_{tot}	$Err.$
CKT1	44K	10K	2	164	15	179	123	11	134	10%	74	7	81	15%
CKT2	67K	18K	2	150	24	174	135	13	148	15%	83	8	91	20%
CKT3	131K	32K	2	181	23	203	159	12	171	12%	114	12	126	17%
CKT4	168K	39K	2	452	186	638	245	52	297	18%	158	34	192	22%
CKT5	256K	78K	2	890	320	1210	494	148	642	11%	255	94	349	16%
CKT6	511K	151K	3	320	779	1099	302	493	795	19%	212	253	468	24%
CKT7	1.0M	300K	2	2023	2035	4058	1534	1225	2759	14%	847	606	1453	19%