Tradeoff Analysis and Optimization of Power Delivery Networks with On-Chip Voltage Regulation

Zhiyu Zeng, Xiaoji Ye, Zhuo Feng*, Peng Li

Department of ECE, Texas A&M University
*Department of ECE, Michigan Technological University
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Outline

- **Motivation**
  - Multiple power islands [Lackey, ICCAD 2002]

- **Overview of on-chip voltage regulation**
  - Introduction to on-chip low-dropout voltage regulators (LDOs)

- **Simulation for power delivery networks with on-chip LDOs**
  - Power delivery network modeling
  - Simulation challenges
  - GPU-CPU combined simulator: GSim

- **Design for power delivery networks with on-chip LDOs**
  - Design aspects
  - Design tradeoffs investigation
  - Optimization formulation
  - Experimental results of optimization scheme for two test circuits

- **Conclusion**
Motivation I

- Power is critical to IC designs
  - Technology scaling leads to larger power consumption/density
  - Power crisis of high-performance processors
  - Growth in low-power SoCs for portable devices

ITRS Roadmap 2009
Motivation II

- **Power consumption of CMOS circuits**
  - Active power: \( P = CV^2f \)
  - Leakage power: sub-threshold current

- **Low-power techniques**
  - Clock gating
  - Power gating
  - Dynamic voltage and frequency scaling (DVFS)
  - Multiple voltage islands (MVI)
Motivation III

- **Multiple voltage Islands**
  - High voltage for I/O buffers (1.8V), medium voltage for analog circuits (1.2-1.4V), low voltage for logic circuits (0.6-1V) [Hazucha, JSSC 2005]
  - High voltage for critical circuit blocks, low voltage for non-critical blocks
  - Require multiple voltage supplies on chip
  - On-board voltage regulator modules (VRMs): space and pins costly, off-chip parasitics

[Shah, ElectronicDesign.com, 2008]
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Voltage Regulators

- **Switching regulators:**
  - Pros: high power efficiency
  - Cons: inductors are hard to integrated on chip

- **Linear regulators:**
  - Pros: easy for on-chip integration, small size, low standby current
  - Cons: power efficiency is constrained by $V_{out}/V_{in}$ ratio
  - Low-dropout voltage regulator (LDO): linear regulator with lowest dropout voltage and improved power efficiency
  - Capacitorless LDOs are attractive for on-chip voltage regulation. [Leung, JSSC 2003] [Milliken, TCASI 2007]
On-Chip LDO Background

- **LDO Topology:** [Milliken, TCASI 2007]

![LDO Circuit Diagram](image)

**Basic concepts:**
- Dropout voltage $V_{\text{drop}}$
- Dropout region and regulation region
- Power efficiency $\varepsilon$: $\varepsilon = \frac{I_{\text{out}}V_{\text{out}}}{I_{\text{in}}V_{\text{in}}} = \frac{I_{\text{out}}V_{\text{out}}}{(I_{\text{out}} + I_p)V_{\text{in}}}$
- Line regulation $\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}}$ and load regulation

[Lee, TI Application Report 1999]
Electrical Characteristics of LDOs

- **Response to $I_{\text{out}}$ variation**

- **Response to $V_{\text{in}}$ variation**
Benefits of On-Chip Voltage Regulation

- **Suppressing high-frequency local droop**
  - LDOs provide strong local voltage regulation

- **Remedying mid-frequency global resonance**
  - The resonance is blocked at the input of voltage regulator
Overview of This Work

- **Simulation for power delivery networks with on-chip voltage regulation**
  - Understand detailed electrical characteristics
  - GPU-CPU combined simulator: Gsim

- **Tradeoff analysis for on-chip voltage regulation**
  - Overall power efficiency
  - Maximum voltage droop
  - LDO overhead

- **Optimization for on-chip voltage regulation**
  - Optimization formulation
  - Observation for two test circuits
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Power Delivery Network with On-Chip LDOs

- **Simulation challenges:**
  - Large on-chip grids with millions nodes. SPICE is not practical.
  - Hundreds to thousands LDOs (nonlinear): existing power grid solvers cannot handle nonlinear devices.

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[Diagram showing Off-Chip and On-Chip Models]
GSim Simulation Framework

- Circuit partitioning relaxation method
GSim Details

- **Circuit partition update scheme**
  - Through partition boundary voltages

- **Convergence**
  - Check the average and maximum voltage changes at partition boundaries
  - Smooth voltage changes on the boundaries
  - Can be improved by multi-level Newton method
GSim Simulation Results

- **GSim is very efficient**
  - Cost of on-chip power grid analysis is dominant. Over 50X speedup over CHOLMOD
  - LDOs are simulated individually, potential parallelism
  - Fast convergence: average <3 iterations per step

<table>
<thead>
<tr>
<th>Num. Nodes</th>
<th>Num. LDOs</th>
<th>Runtime (s)</th>
<th>Num. Iteration</th>
</tr>
</thead>
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<tr>
<td></td>
<td></td>
<td>Total /Step</td>
<td>CPU %</td>
</tr>
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<td>1810 1.6</td>
<td>22</td>
</tr>
<tr>
<td>2.25M</td>
<td>144</td>
<td>1768 1.5</td>
<td>23</td>
</tr>
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<td>9M</td>
<td>64</td>
<td>7398 6.2</td>
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</tr>
<tr>
<td>9M</td>
<td>256</td>
<td>4500 3.7</td>
<td>27</td>
</tr>
</tbody>
</table>
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Design Aspects I

- Design aspects for on-chip voltage regulation:
  - Maximum voltage droop
  - Overall power efficiency
  - LDO overhead
Design Aspects II

- **Intermediate variables:**
  - Number of LDOs.
  - Input voltage.

- **Maximum voltage droop:**
  - Maximum voltage droop vs. number of LDOs
  - Maximum voltage droop vs. input voltage

- **Overall power efficiency:**
  - Overall power efficiency vs. number of LDOs
  - Overall power efficiency vs. input voltage

- **LDO overhead:**
  - Chip area
  - Routing resources
  - In proportion to number of LDOs
Maximum Voltage Droop I

- Maximum voltage droop vs. number of LDOs
  - More LDOs, stronger local voltage regulation
  - More LDOs, less amount of dynamic current for each LDO
  - Increasing number of LDOs would lower maximum voltage droop
Maximum Voltage Droop II

- **Maximum voltage droop vs. input voltage**
  - In regulation region, voltage droop is stable
  - In dropout region, voltage droop increases with decreasing input voltage
  - Significantly lowering the input voltage is harmful

![Maximum Voltage Droop vs. Input Voltage](image_url)
Power Efficiency I

- **Overall power efficiency**  
  \[ \varepsilon = \frac{\sum_{k=1}^{N} P_k^o}{\sum_{k=1}^{N} P_k^i} \]

- **Power efficiency vs. number of LDOs**
  - Quiescent current \( I_q \) is small
  - Reducing LDOs has little impact on power efficiency

![Power Efficiency vs. Number of LDOs](image-url)
Power Efficiency II

- **Power efficiency vs. input voltage**
  - Less $V_{in}$, larger $\frac{V_{out}}{V_{in}}$
  - In the drop-out region, LDO works as a resistor
  - Lowering input voltage significantly increases power efficiency
Design Tradeoffs

- Power efficiency $\uparrow$ vs. input voltage $\downarrow$
- Voltage droop $\downarrow$ vs. $\#$ LDOs $\uparrow$ and input voltage $\uparrow$
- LDO overhead $\downarrow$ vs. $\#$ LDOs $\downarrow$

![Diagram showing power efficiency and voltage droop tradeoffs](image)

- Regulation Region
- Dropout Region

- $V_{in}=1.65V$
- $V_{in}=1.4V$

- $N=4$
- $N=9$
- $N=16$
- $N=25$
Optimization for On-Chip Voltage Regulation

- **Notations:**
  - $N$ power islands, each has $X_k \times Y_k$ LDOs

- **Objective function (maximize power efficiency):**
  \[
  \mathcal{E} = \frac{\sum_{i=1}^{N} \sum_{j=1}^{X_k Y_k} P_{ij}^o}{\sum_{i=1}^{N} \sum_{j=1}^{X_k Y_k} P_{ij}}
  \]

- **Subject to:**
  - Voltage droop constraint: $v_k^d \leq v_k^m$, $k = 1, \ldots, N$
  - Overhead constraint: $\sum_{k=1}^{N} X_k Y_k \leq M$

- **Optimization variables:**
  - number of LDOs $(X_k, Y_k)$ and input voltage $(V_{in})$
Optimization Using APPS

- Asynchronous parallel pattern search (APPS) [Gray, TMS 2006]
  - Solve unconstrained and bound-constrained optimization problems
  - Simulation based optimization

- Optimization formulation
  - Objective function: \( f(x) = 1 - \varepsilon + P(V_d) + P(XY) \)
  - Constraints: \( 1 \leq \{x_1, \ldots, x_N\}, 1 \leq \{y_1, \ldots, y_N\}, 0 \leq V_{in} \)
  - Penalty function \( P(V_d) \) for voltage droop constraint:
    \[
    P(V_d) = \begin{cases} 
    \alpha(V_d^m - V_i^d)^2, & \exists i : V_d^i > V_i^d \\
    0, & \text{others}
    \end{cases}
    \]
  - Penalty function \( P(XY) \) for overhead constraint:
    \[
    P(XY) = \begin{cases} 
    \beta(\sum_{k=1}^{N} X_k Y_k - M)^2, & \sum_{k=1}^{N} X_k Y_k > M \\
    0, & \sum_{k=1}^{N} X_k Y_k < M
    \end{cases}
    \]
Experimental Setups- Optimization

- **Two test circuits:**
  - Circuit 1: low-voltage dominant
  - Circuit 2: high-voltage dominant

<table>
<thead>
<tr>
<th>Domain</th>
<th>J</th>
<th>$V_{dd}$ (V)</th>
<th>$V_m$ (V)</th>
<th>Area</th>
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<tbody>
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<td>1.4</td>
<td>70m</td>
<td>1</td>
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<tr>
<td>B</td>
<td>1/2</td>
<td>1.2</td>
<td>60m</td>
<td>2</td>
</tr>
<tr>
<td>C</td>
<td>1/3</td>
<td>1.0</td>
<td>50m</td>
<td>6</td>
</tr>
</tbody>
</table>
Experimental Results - Optimization I

- **Circuit 1:**
  - Island C has the dominant current loads
  - Island C has the tightest voltage droop constraint
  - Most of the LDOs are placed in island C
  - Input voltage is low and overall power efficiency is low
  - The voltage regulators in A are pushed towards dropout region
  - Voltage regulators in B and C are away from dropout region
  - May need new voltage regulation topologies to increase the overall power efficiency [Amelifard, TCAD 2009]

<table>
<thead>
<tr>
<th>Test Circuit</th>
<th>M</th>
<th>Num. LDOs</th>
<th>$V^d$ (V)</th>
<th>$V_{in}$ (V)</th>
<th>$\varepsilon$ %</th>
<th>Runtime (h)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Total</td>
<td>A</td>
<td>B</td>
<td>C</td>
<td>A</td>
</tr>
<tr>
<td>1</td>
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<td>48</td>
<td>4</td>
<td>8</td>
<td>36</td>
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<td>54</td>
<td>6</td>
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<td>69.6m</td>
</tr>
</tbody>
</table>
### Experimental Results - Optimization II

- **Circuit 2:**
  - Domain A has the dominant current loads
  - Most of the LDOs are placed in island A
  - Input voltage is high and overall power efficiency is high
  - The voltage regulators in A, B and C are all away from dropout region

<table>
<thead>
<tr>
<th>Test Circuit</th>
<th>M</th>
<th>Num. LDOs</th>
<th>V\text{d} (V)</th>
<th>V\text{in} (V)</th>
<th>(\varepsilon) %</th>
<th>Runtime (h)</th>
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<tr>
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Conclusion

- **Gsim for power delivery network simulation**
  - Fast GPU-CPU combined simulation
  - Handle nonlinearity of LDOs in the network
  - Provide detailed electrical characteristics of LDOs in the network

- **Survey on design aspects of on-chip power regulation**
  - Maximum voltage droop
  - Overall power efficiency
  - LDO overhead
  - Tradeoffs among these three aspects

- **Optimization scheme for on-chip power regulation**
  - Optimization formulation
  - Key observations for two test circuits
Thanks!