Logic Description

For: 115 kV Line Panel Standard Design
One Breaker Normal Length Line Panel with New Panels at All Ends

The primary relay includes the following basic functions:

- Primary Line Protection Functions
- Line Breaker Reclosing
- Line Breaker Close Supervision
- Recloser Mode Selection
- Analog Metering
- Line Breaker Failure Logic
- Primary Breaker Trip Coil and 86BF Lockout Relay Coil Monitoring
- Primary Trip and 86BF Output Contact Testing
- Analog-Digital (A-D) Calibration Test Alarming
- Carrier Check-Back Functions
- Self-Testing and Monitoring
- Oscillographic Fault Recording
- Sequence Of Events Recording

The secondary relay includes the following basic functions:

- Secondary Line Protection Functions
- Breaker Trip Coil Monitoring
- Secondary Trip Output Contact Testing
- Self-Testing and Monitoring
- Oscillographic Fault Recording
- Sequence Of Event Recording

Primary line protection:

The primary line protection functions include directional comparison blocking (DCB) using on-off carrier and direct tripping functions. The DCB function includes zone 2, forward looking, elements which are used to initiate DCB tripping. They include phase (M2P) and ground (Z2G) mho elements and a ground directional overcurrent (67G2) element. These are set to detect faults anywhere on the line and to detect faults behind the remote breaker, which trip the remote breaker (see Figure P-1). This setting may be longer than the traditional zone 2 setting as required for tripping during a remote line breaker failure condition (see "Line Breaker Failure Logic" below).

The blocking functions key the carrier to block remote end tripping during reverse faults. They include a non-directional ground overcurrent element and zone 3, reverse looking, phase mho (M3P), ground mho (Z3G) and ground directional overcurrent (67G3) elements. The reverse blocking elements are coordinated with the remote forward tripping elements such that no remote breaker DCB tripping occurs during reverse faults as long as the carrier is active (see figure P-1). Load encroachment logic may be required to block the forward phase (M2P) and reverse phase (M3P) mho elements from operating on through load.

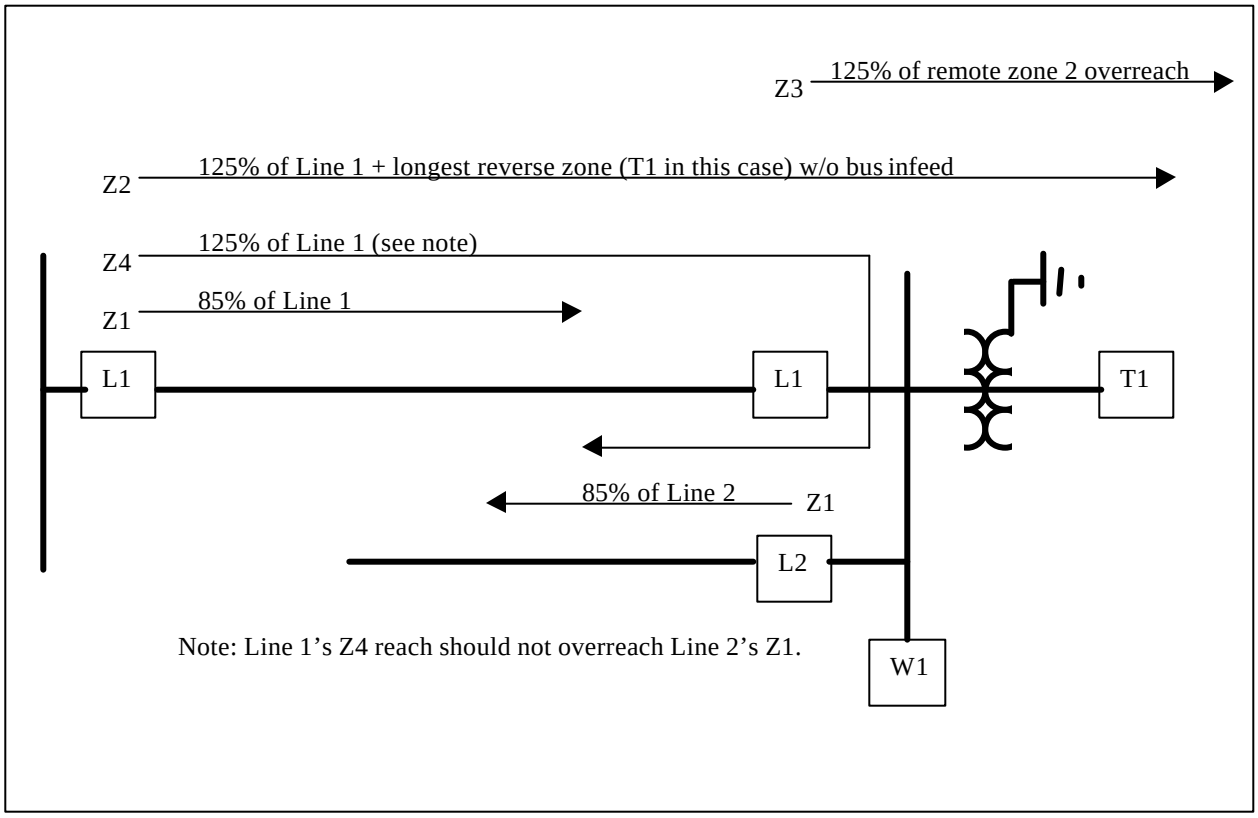

Figure P-1: Typical primary relay zone settings

The non-directional ground overcurrent blocking element is used to provide faster keying of the blocking transmitter. During forward faults, the forward directional ground overcurrent elements provide a STOP output from the DCB logic to override the non-directional start (NSTRT) output.

Operation of the 86BF lock-out relay (IN203) will start carrier for 5 cycles, if the carrier was not already operating. It will also stop carrier after the 5 cycles or if it was already operating. This is intended to facilitate fast tripping of the remote line breaker(s) following a breaker failure operation and assure that they do not reclose. See "Line Breaker Failure Logic" below for more details.

The 43/85 is used to disable DCB functions. Turning the 43/85 OFF deasserts IN106 which, in turn, asserts the BT input to the DCB logic (simulating receipt of a continuous block) and prevents carrier keying (OUT104) from reverse blocking elements and checkback.

Direct tripping functions include instantaneous tripping mho (M1P and Z1G) and non-directional instantaneous overcurrent (50P1 and 50G1) elements, time delayed mho (M4PT and Z4GT), ground directional time overcurrent (51S1T) and out-of-step trip (OST) elements. The non-directional instantaneous overcurrent elements can only be applied if the bus's contribution to a close-in line fault is larger than the line's contribution to a bus fault. The out-of-step trip element will only be applied as required by power system dynamic performance studies. The zone 4 mho elements are used for time delayed direct tripping, since the zone 2 pilot tripping elements may have settings that are longer than can be tolerated for time delayed direct tripping.

Switch onto fault logic is also provided for the case of line connected VTs. In this case, the MHO and directional elements may not operate reliably if the line breaker is closed into a faulted line. Phase (50P2) and ground (50G4) instantaneous overcurrent elements are used to initiate the SOTF trip.

Reclosing

The SEL-421-1 reclosing logic is used to reclose the line breaker. Reclosing is initiated (3PRI) for primary and secondary relay trips (3PT) except switch onto fault trips (SOTFT) if the 43/79 is in AUTO (IN202). The secondary reclose initiate is brought into the primary relay via mirrored bits communication (RMB1A).

The breaker close output of the recloser (BK1CL) is blocked, after the open interval timer times out, by the breaker close supervision (3P1CLS) until the correct voltage and synchronism conditions (A1, A2 or Asynch) exist (see "Recloser Mode Selection" below). Since the recloser stops after the open intervsal timer times out, a 5 second (300 cycle) timer is added on each of the hot functions (timers PCT03 for Hot Bus, PCT04 for Hot Line and PCT05 for synchrocheck) to delay the close output after the voltage conditions are met.

The close output is unlatched (ULCL1) when the breaker closes (52AA1).

The recloser will go to the lock-out mode anytime the breaker opens without a reclose initiate (3PRI) present. It will also go to lock-out anytime the drive-to-lock-out input (79DTL) is asserted (see "Line Breaker Failure Logic" below). Once in lock-out, the recloser will stay in lock-out until the drive-to-lock-out input (79DTL) is deasserted and the breaker is closed for the reclaim (reset) time delay.

An alarm output (OUT213) is asserted when the recloser is in lock-out (Relay Word bit BK1LO), the breaker is open (NOT 52AA1) and the 43/79 is in AUTO (IN202). The target light (79LO) is programmed with the same logic and will only light when the alarm output (OUT213) is asserted.

Line Breaker Close Supervision

Output OUT208 is used to supervise the SCADA and manual line breaker close. It is programmed to close if the bus or line is dead or if they are both hot and in synchronism. In most applications, this output is jumpered externally to provide unsupervised SCADA close, but, the logic for the output is programmed anyway.

Recloser Mode Selection

The recloser mode selection (A1, A2 or Asynch) is accomplished by pulsing remote bits RB01, RB02 or RB03 respectively via comm port. Protection timers PCT06, PCT07 and PCT08 stretch the remote bit pulses to 10 cycles. This is required to assure that the mode selection logic, located in the automation section of the 421-1 relay, detects the remote bit pulse which only lasts for one scan of the protection logic. The mode is based on the position of latches ALT01 and ALT02. If both are reset, then the mode is Asynch (synchrocheck close only). If ALT01 is set, the mode is A1 (Hot Bus – Dead Line or synchrocheck). If ALT02 is set, the mode is A2 (Dead Bus – Hot Line or synchrocheck). ALT01 and ALT02 are never set at the same time.

Pulsing RB01 when latch ALT01 is reset will set latch ALT01 and reset latch ALT02. This is the A1 mode which allows reclose for Hot Bus – Dead Line or synchrocheck. If the bus is hot (>85% of the bus B-N input voltage) and the line is dead (<50% of the line B-N input voltage), then the SEL variable ASV004 will assert and assert the recloser close supervision (3P1CLS), allowing the recloser to close the line breaker. If the bus and lines are both hot and in synch, then the synchrocheck logic output 25A1BK1 will assert and assert the recloser close supervision (3P1CLS) after time delay PCT05, allowing the recloser to close the line breaker. Pulsing RB01 when latch ALT01 is set will reset latch ALT01, placing the recloser in the Asynch mode.

Pulsing RB02 when latch ALT02 is reset will set latch ALT02 and reset latch ALT01. This is the A2 mode which allows reclose for Dead Bus – Hot Line or synchrocheck. If the bus is dead (<50% of the bus B-N input voltage) and the line is hot (>85% of the line B-N input voltage), then the SEL variable ASV005 will assert and assert the recloser close supervision (3P1CLS), allowing the recloser to close the line breaker. If the bus and lines are both hot and in synch, then the synchrocheck logic output 25A1BK1 will assert and assert the recloser close supervision (3P1CLS) after time delay PCT05, allowing the recloser to close the line breaker. Pulsing RB01 when latch ALT02 is set will reset latch ALT02, placing the recloser in the Asynch mode.

Pulsing RB03 when either latch ALT01 or ALT02 is set will reset latch ALT01 (if it is set) and reset latch ALT02 (if it is set). This is the Asynch mode which allows reclose for synchrocheck only. If the bus and lines are both hot and in synch, then the synchrocheck logic output 25A1BK1 will assert and assert the recloser close supervision (3P1CLS) after time delay PCT05, allowing the recloser to close the line breaker. Pulsing RB03 when latches ALT01 and ALT02 are both reset will set latch ALT01, placing the recloser in the A1 mode.

Note that the synch-check logic is allowed to operate continuously, even when the breaker is closed by setting the block-synch input (BSYNCH1) to a logical "0". This is done to facilitate phase angle measurement. See "Analog Metering" below for more information.

Analog Metering

Various analog metering values are provided to the substation RTU for SCADA remote monitoring. Typically, line MW, MVAR, V and A are read by the RTU.

The phase angle (PA) of the voltage across the line breaker is also available from the breaker 1 synch-check logic (ANG1DIF). Traditionally, synch-check functions only operate when the associated breaker is open. When the breaker is closed, the voltage angle across it is "0". The synch-check logic of the 421-1 returns an angle value of "999" anytime it is blocked from operating. For this reason, the block-synch input (BSYNCH1) is set to a logical "0", allowing the logic to run continuously, returning a correct value of "0" when the breaker is closed. The RTU can not read the value of ANG1DIF directly, either by DNP or through the 2030. However, it can read the value of the first few automation math variables (AMV001-AMV032 for DNP and AMV001-AMV004 for 2030 applications). For this reason, the whole number value (FLOOR function) of the phase angle value (ANG1DIF) is stored in the first automation math variable (AMV001 = FLOOR(ANG1DIF)). The FLOOR function returns the next whole number smaller than the ANG1DIF (if ANG1DIF = 8.354 then FLOOR(ANG1DIF) = 8.000, if AND1DIF = -4.357 then FLOOR(ANG1DIF) = -5.000). The value of AMV001 can not be viewed directly so the same value is also stored in AMV254 which can be viewed with the "MET AMV" command.

"LINE HOT" indication is provided on the front of the relay using push button 1's LED (upper left) anytime the line voltage is greater than 25% of it's nominal value.

Line Breaker Failure Logic

The line breaker failure logic is initiated internally by a 3 pole trip in the primary relay (3PT) and externally by the secondary relay and other external trips (bus lock-out, TT received, etc) through an external breaker failure initiate input (IN103). The logic runs a timer any time the breaker is closed (as sensed by current through the breaker) and there is an initiate present. If the breaker does not open within the time delay, a breaker failure is declared and the logic output (BFTRIP1) asserts OUT103 to operate the 86BF lock-out relay.

For installations with gas insulated breakers, the low-gas pressure block-trip in the breaker asserts IN207 whenever the breaker is in block-trip. IN207 asserts the breaker failure trip (BFTR1) without waiting for the breaker failure timer if the breaker failure logic is initiated (BFI3P1) and the breaker is closed (as determined by the breaker failure overcurrent fault detectors 50FA1, 50FB1, 50FC1 or 50R1).

The status of the 86BF lock-out is read on IN203 (“86BF OPERATED”). This input is used for the 86BF coil monitoring (see “Primary Breaker Trip Coil and 86BF Lock-out Relay Coil Monitoring” below) and as a part of the breaker failure logic to allow fast clearing of the remote end line breaker(s) and to assure that they do not automatically reclose.

Following a breaker failure of the local line breaker, if the initiating fault was a line fault, the remote line breaker(s) will be open and the carrier will not be operating. When the 86BF operates, IN203 will assert and the carrier will be started for 5 cycles (timer PCT02). Carrier received at the remote line terminal(s) will drive the remote line breaker recloser(s) to lock-out (79DTL asserts if carrier is received for more than 3 cycles and the breaker is open).

Following a breaker failure of the local line breaker, if the initiating fault was a reverse fault (bus or transformer), the remote line breaker(s) will be closed and the carrier will be operating. When the 86BF operates, IN203 will assert and the carrier will be stopped. When the carrier stops, the remote line breaker(s) will trip by directional comparison blocking after a short coordination delay (zone 2 tripping elements are set to overreach the longest reverse zone – see “Primary Line Protection” above). When the remote line breaker(s) open the remote line breaker recloser(s) will be driven to lock-out (79DTL asserts if the breaker opens within 300 cycles of receiving carrier).

Primary Breaker Trip Coil and 86BF Lockout Relay Coil Monitoring

The trip coil monitor logic provides an alarm any time the status of the breaker (52AA1/IN101) does not match the status of the trip coil monitor input (IN104) that is reading negative through the breaker trip coil. If the breaker is closed (52a closed and status input asserted), the trip coil monitor input should be asserted. Conversely, if the breaker is open (52a open and status input deasserted), the trip coil monitor input should be deasserted. The logic detects a violation of either of these conditions. A timer (AST01) is provided to allow for transitions during breaker opening and closing.

The trip coil monitoring logic is inhibited during output contact testing to prevent false alarms (see "Primary Trip and 86BF Output Contact Testing" below).

The 86BF coil monitor logic provides an alarm any time the status of the 86BF lock-out relay (86BF Operated/IN203) does not match the status of the 86BF coil monitor input (IN201) that is reading negative through the 86BF lock-out relay coil. If the 86BF lock-out relay is reset (status input deasserted), the 86BF coil monitor input should be asserted. Conversely, if the 86BF lock-out relay is operated (status input asserted), the 86BF coil monitor input should be deasserted. The logic detects a violation of either of these conditions. A timer (AST07) is provided to allow for transitions during 86BF lock-out relay operation.

The 86BF coil monitoring logic is inhibited during output contact testing to prevent false alarms (see "Primary Trip and 86BF Output Contact Testing" below).

Primary Trip and 86BF Output Contact Testing

Critical output contacts, including breaker trip and 86BF operate contacts, are exercised every 25 hours in both the primary and secondary relays. The timing of the tests are determined by the primary relay. Each contact is tested in sequence, starting with the primary relay line breaker trip output followed by the primary relay 86BF operate output and, lastly, the secondary relay breaker trip output. A mirrored bit is used to initiate the testing in the secondary relay.

The timing circuit consists of an automation counter (ACN03) that increments its count each day at midnight when the SELogic hour variable (THR) equals 0. The counter counts from 0 to 23 and then resets itself back to 0. 1 is added to the current count (AMV255 = ACN03CV +1) which results in a count value that ranges from 1 to 24 and then resets to 1. A test sequence is initiated by automation SEL variable ASV065, each time AMV255 equals the current hour (THR). The value of AMV255 can be viewed with the "MET AMV" command to determine the time of the next test. A test can also be manually initiated by pulsing remote bit RB08. Protection timer PCT11 stretches the remote bit pulse to 10 cycles. This is required to assure that the I/O test initiate logic, located in the automation section of the 421-1 relay, detects the remote bit pulse which only lasts for one scan of the protection logic. The raw counter count (ACN03CV) is also used to initiate a check back sequence (see "Carrier Check-Back Functions" below).

The test sequence is initiated when SEL variable ASV065 asserts or when remote bit RB08 asserts which, in turn, asserts SEL variable ASV064 which seals itself in for the duration of the test. ASV064 blocks the trip coil and 86BF coil monitoring logic (see "Primary Breaker Trip Coil and 86BF Lockout Relay Coil Monitoring" above) and runs automation sequencing timer AST03 which controls the output contact testing sequence.

The table below shows the timing sequence for the output testing:

Step No.	**Time (sec)**	**Action**	**Associated Relay Word bit**
1	0	Block trip and 86BF coil monitoring logics.	ASV064
Steps 2 through 12 test the line breaker trip output			
2	0	Isolate the line breaker trip output with OUT106 if the line breaker trip coil monitor input (IN104) is asserted.	ASV051 OUT106
3	0 +	Line breaker trip coil monitor input (IN104) deasserts.	IN104
4	0 ++	Assert OUT201 to transfer the line breaker trip output to the test resistor.	ASV052 OUT201
5	0 +++	Line breaker trip coil monitor input (IN104) asserts.	IN104
6	0.5	Assert line breaker trip output (OUT101)	ASV053 OUT101
7	0.5 +	Line breaker trip coil monitor input (IN104) deasserts.	IN104
8	1.0	Assert line breaker trip output test alarm bit (ASV054) for a failure of any of the above steps.	ASV066 ASV054
9	1.0 +	Set the alarm latch (ALT04) and deassert the alarm output (OUT215) if test resulted in an alarm (step 8).	ALT04 OUT215

10	1.5	Deassert the line breaker trip output (OUT101).	ASV053 OUT101
11	2.0	Deassert OUT201 to return the line breaker trip output to the trip coil circuit.	ASV052 OUT201
12	2.0 +	Deassert OUT106 to reconnect the line breaker trip output to the trip coil.	ASV051 OUT106
Steps 13 through 23 test the 86BF trip output			
13	6.0	Isolate the 86BF trip output with OUT108 if the 86BF trip coil monitor input (IN201) is asserted.	ASV059 OUT201
14	6.0 +	86BF trip coil monitor input (IN201) deasserts.	IN201
15	6.0 ++	Assert OUT203 to transfer the 86BF trip output to the test resistor.	ASV060 OUT203
16	6.0 +++	86BF trip coil monitor input (IN201) asserts.	IN201
17	6.5	Assert 86BF trip output (OUT103)	ASV061 OUT103
18	6.5 +	86BF trip coil monitor input (IN201) deasserts.	IN201
19	7.0	Assert 86BF trip output test alarm bit (ASV062) for a failure of any of the above steps.	ASV068 ASV062
20	7.0 +	Set the alarm latch (ALT04) and deassert the alarm output (OUT215) if test resulted in an alarm (step 30).	ALT04 OUT215
21	7.5	Deassert the 86BF trip output (OUT103).	ASV061 OUT103
22	8.0	Deassert OUT203 to return the 86BF trip output to the trip coil circuit.	ASV060 OUT203
23	8.0 +	Deassert OUT108 to reconnect the 86BF trip output to the trip coil.	ASV059 OUT108
Steps 24 and 25 sequence the trip output testing in the 21S relay			
24	9.0	Assert transmitted mirrored bit TMB1A to initiate a secondary breaker trip output test (see "Secondary Trip Output Contact Testing" below.	TMB1A
25	9.5	Deassert transmitted mirrored bit TMB1A.	TMB1A
The remaining steps complete the test sequence			
26	16.0	Trip output testing sequence timer (AST03) reaches its preset value, breaks the testing sequence seal in and resets itself.	AST03Q ASV064 AST03IN AST03R
27	16.0 +	Release trip and 86BF coil monitoring logics.	ASV064

Analog-Digital (A-D) Calibration Test Alarming

The instantaneous primary values of relay voltage (Van, Vbn, Vcn) and line current (Ia, Ib, Ic) in the primary relay are compared by the SEL-2030 communications processor to the corresponding values in the secondary relay to detect analog-digital (A/D) converter drift or failure. If both relays are functioning properly, the values should be within a reasonable tolerance (8%) of each other.

Each time the 2030 runs a comparison test (approximately once a second), it tells the 21P relay if the test was successful (all 6 values are within tolerance) or if it failed (one or more of the values are out of tolerance) by pulsing a pair of remote bits in the 21P (RB05 for a good test and RB06 for a failed test). The 21P runs a count-up/count-down counter to accumulate failed tests. Counter ACN01 functions as the count-down counter by counting the successful tests. Counter ACN02 functions as the count-up counter by counting the failed tests. If the net count (count-up minus count-down) exceeds 10 an "Analog I/O Test Fail" alarm is generated by asserting SEL variable ASV063. If the net count reaches zero or less, or, if either counter's count value reaches 100, the count values in both counters are reset to zero.

Carrier Check-Back Function

The 21P relay is programmed to function as a master check-back terminal or as a slave terminal. Math variable AMV002 stores a check-back function code that determines the check-back mode as follows:

Function Code (F)	Check-back Function
0	no check-back
1	master check-back for 2 terminal line
2	master check-back for 3 terminal line
3	slave check-back terminal #1
4	slave check-back terminal #2

If the 21P is set-up as a master (function code "F" = 1 or 2), the day counter (ACN03) described in "Primary Trip and 86BF Output Contact Testing" is used by the master check-back logic to initiate a check-back every 25 hours. A time adder (T) can be used to prevent all the lines in the station from initiating a check-back at the same time (AMV256 = ACN03CV + T). The value of AMV256 can be viewed with the "MET AMV" command to determine the time of the next check-back. A check-back is also initiated each time the 43/85 is turned on.

Once initiated, the master check-back runs a sequencing timer (AST04) which control the steps involved in the check-back as follows:

Step No.	Time (sec)	Action	Associated Relay Word bit
1	0	Master check-back is initiated (ASV082 and ASV083) either by the day counter (ASV084) or by turning the 43/85 on (IN106).	ASV082 ASV084 IN106
2	0	Sequencing timer AST04 runs	ASV083
3	5	Reset check-back received latches ALT05 and ALT06 and check-back alarm latch ALT07.	ALT05 ALT06 ALT07
4	5 - 11	Key carrier	ASV076 OUT104
Step 5 looks for an echo back from slave terminal #1			
5	12 - 22	Set check-back received latch ALT05 if carrier is received (assumed to be from terminal #1) during this period.	ALT05 IN107
Step 6 looks for an echo back from slave terminal #2 (if this is a 3 terminal line)			
6	24 - 30	Set check-back received latch ALT06 if carrier is received (assumed to be from terminal #2) during this period.	ALT06 IN107
7	35	Assert check-back fail SEL variables ASV077 (terminal #1) and/or ASV078 (terminal #2) if the check-back was not successful.	ASV077 ASV078
8	35	Set check-back alarm latch ALT07 and assert alarm output OUT212 if either check-back fail SEL variable is asserted.	ALT07 OUT212
9	40	Reset check-back sequencing timer AST04 and reset the master check-back logic. Note that check-back received latches ALT05 and ALT06 do not reset at this time (see step 3)	ASV083 AST04Q ASV077 ASV078

Once a check-back fail alarm is asserted, it can only be reset by initiating a new check-back (step 3 above) or by asserting remote bit RB07 (this is intended for technician use during testing). Protection timer PCT10 stretches the remote bit pulse to 10 cycles. This is required to assure that the I/O test initiate logic, located in the automation section of the 421-1 relay, detects the remote bit pulse which only lasts for one scan of the protection logic.

If the 21P is set-up as a slave (Function code "F" = 3 or 4), a check-back echo is initiated any time the carrier is keyed for more than 2 seconds as follows:

Step No.	**Time (sec)**	**Action**	**Associated Relay Word bit**
1	0	Carrier is received (IN107 asserts) and starts check-back slave sequencing timer AST06.	IN107
2	< 2	Check-back slave sequencing timer AST06 resets if carrier stops (IN107 deasserts).	IN107
3	2	Check-back slave sequencing timer AST06 seals in.	
If this is check-back slave terminal #1 (F = 3)			
4	10 - 17	Key carrier.	ASV079 ASV081 OUT104
If this is check-back slave terminal #2 (F = 4)			
4	19 - 26	Key carrier.	ASV080 ASV081 OUT104

If carrier is received continuously for more than 30 seconds, timer AST05 times out (AST04Q asserts) and asserts the check back alarm output (OUT212). The alarm will clear when the carrier stops.

Self-Testing and Monitoring

The 21P contains self checking logic to exercise the microprocessor's hardware and software. It also monitors the voltage applied to the relay and generates a loss of potential (LOP) alarm if one or more of the voltages are out of range. All of the primary relay failure alarms are alarmed through one "PRIMARY RELAY (TROUBLE)" alarm output (OUT215) as follows:

1. Software failure (SALARM)
2. Hardware failure (HALARM)
3. Loss of potential (LOP)
4. Loss of DC to the relay
5. Line breaker trip coil monitor fail (AST01Q and ALT04)
6. 86BF coil monitor fail (AST07Q and ALT04)
7. Line breaker trip output contact test fail (ASV054 and ALT04)
8. 86BF trip output contact test fail (ASV062 and ALT04)

Items 5 through 8 operate alarm latch ALT04 and can only be reset by pulsing remote bit RB04. This is designed to require a qualified person to access the relay, either locally or remotely, to determine the cause of the failure and appropriate action. Protection timer PCT09 stretches the remote bit pulse to 10 cycles. This is required to assure that the I/O test initiate logic, located in the automation section of the 421-1 relay, detects the remote bit pulse which only lasts for one scan of the protection logic.

When the Analog-digital calibration test fails (ASV063 and ALT08), there is no way of telling which relay has A/D calibration problems. For this reason, it is alarmed through a general purpose "XX LINE RELAY MAINTENANCE (REQUIRED)" alarm (OUT209). Failure of the mirrored bit communication link between the 21P and 21S relays (RBADA) is also alarmed through the "XX LINE RELAY MAINTENANCE (REQUIRED)" alarm. ALT08 and can only be reset by pulsing remote bit RB09. This is designed to require a qualified person to access the relay, either locally or remotely, to determine the cause of the failure and appropriate action. Protection timer PCT12 stretches the remote bit pulse to 10 cycles. This is required to assure that the I/O test initiate logic, located in the automation section of the 421-1 relay, detects the remote bit pulse which only lasts for one scan of the protection logic.

Oscillographic Fault Recording

The 21P relay automatically captures an oscillographic record of the currents, voltages and internal relay data for all trips initiated from the primary relay.

Sequence Of Events Recording

The time stamped status of selected discrete data in the primary relay is written to the sequence of events record. This is a first-in-first-out list of the most recent 500 status change events.

Secondary line protection:

The secondary line protection direct tripping functions include instantaneous tripping mho (M1P and Z1G) and non-directional instantaneous overcurrent (50P1 and 50G1) elements and time delayed mho (M2PT and Z2GT) and ground directional time overcurrent (51GT) elements. The non-directional instantaneous overcurrent elements can only be applied if the bus's contribution to a close-in line fault is larger than the line's contribution to a bus fault. The zone 2 mho elements are used for time delayed direct tripping (see figure S-1).

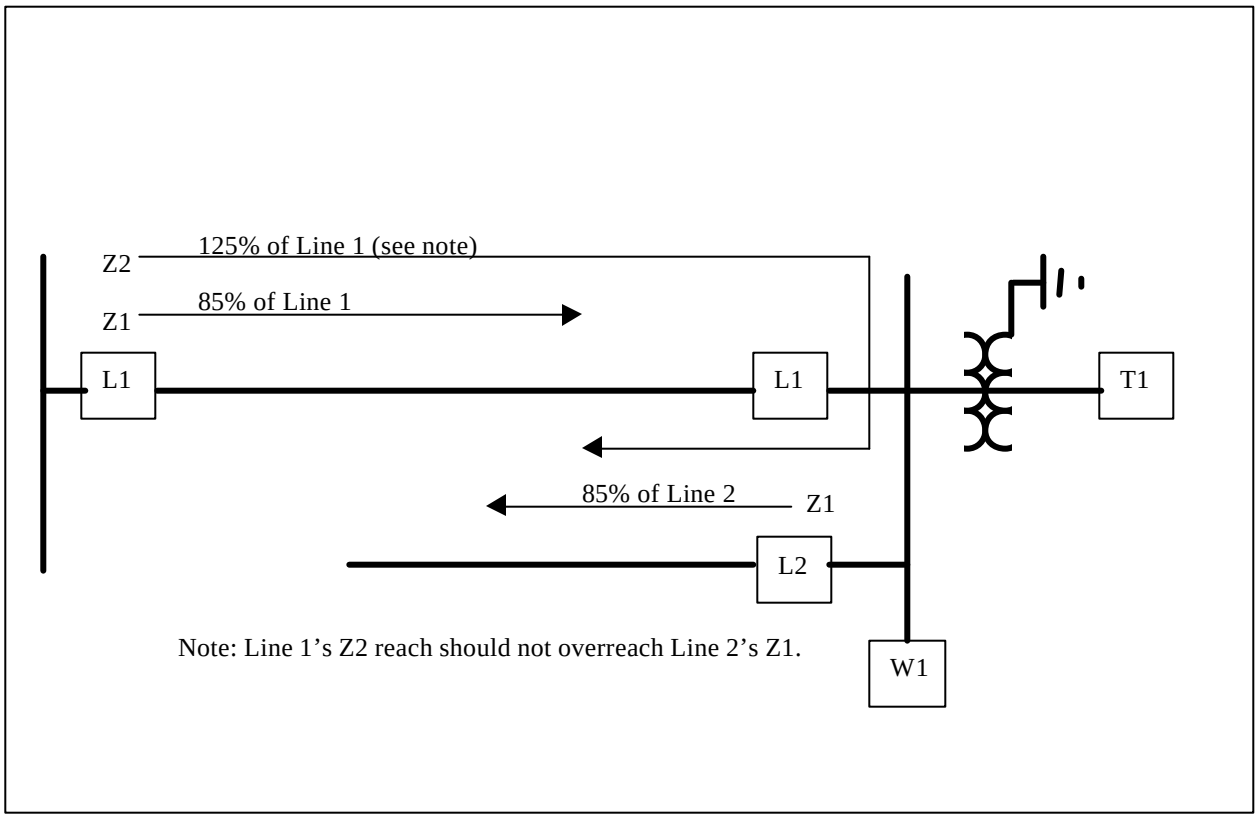

Figure S-1: Typical secondary relay zone settings

Switch onto fault logic is also provided for the case of line connected VTs. In this case, the MHO and directional elements may not operate reliably if the line breaker is closed into a faulted line. Phase (50P2) and ground (50G4) instantaneous overcurrent elements are used to initiate the SOTF trip.

Secondary Breaker Trip Coil Monitoring

The trip coil monitor logic provides an alarm any time the status of the breaker (IN101) does not match the status of the trip coil monitor input (IN103) that is reading negative through the breaker trip coil. If the breaker is closed (52a closed and status input asserted), the trip coil monitor input should be asserted. Conversely, if the breaker is open (52a open and status input deasserted), the trip coil monitor input should be deasserted. The logic detects a violation of either of these conditions. A timer (SV1) is provided to allow for transitions during breaker opening and closing.

The trip coil monitoring logic is inhibited during output contact testing to prevent false alarms (see "Secondary Trip Output Contact Testing" below).

Secondary Trip Output Contact Testing

Breaker trip output contacts are exercised every 25 hours in both the primary and secondary relays. The timing of the tests are determined by the primary relay (see "Primary Trip and 86BF Output Contact Testing" above). Each contact is tested in sequence, starting with the primary relay line breaker trip output followed by the primary relay 86BF operate output and, lastly, the secondary relay breaker trip output. Mirrored bits are used to initiate the testing in the secondary relay.

The test sequence in the secondary relay is initiated when received mirrored bit RMB1A asserts which asserts SEL variable/timer SV3 for 120 cycles (2 seconds). SV3T blocks the trip coil monitoring logic (see "Secondary Breaker Trip Coil Monitoring" above) and initiates the output contact testing sequence.

The table below shows the timing sequence for the output testing:

Step No.	**Time (sec)**	**Action**	**Associated Relay Word bit**
1	0 – 9.0	Primary relay tests it's own output contacts (see "Primary Trip and 86BF Output Contact Testing" above)	
Steps 2 through 14 test the line breaker trip output			
2	9.0	Primary relay asserts (via mirrored bits) secondary relay's received mirrored bit RMB1A which asserts SEL variable/timer SV3.	RMB1A SV3 SV3T
3	9.0	SV3T blocks line breaker trip coil monitoring logic and asserts SEL variable/timer SV6.	SV3T SV6
4	9.0	Isolate the linebreaker trip contact with OUT104 if the line breaker trip coil monitor input (IN103) is asserted.	OUT104
5	9.0 +	Line breaker trip coil monitor input (IN103) deasserts.	IN103
6	9.0 ++	Assert OUT103 to transfer the line breaker trip output to the test resistors.	OUT103
7	9.0 +++	Line breaker trip coil monitor input (IN103) assert and SEL variable/timers SV4 asserts.	IN103 SV4
8	9.5	SEL variable/timers SV4 times out and asserts SEL variable SV5 and line breaker trip output (OUT101)	SV4T SV5 OUT101
9	9.5 +	Line breaker trip coil monitor input (IN103 deasserts.	IN103

10	10.0	SEL variable/timer SV6 times out and asserts line breaker trip output test alarm bit (SV7) for a failure of any of the above steps.	SV6T SV7
11	10.0 +	Set the alarm latch (LT1) and assert the alarm output (OUT107) if test resulted in an alarm (step 10).	LT1 OUT107
12	10.25	SEL variable/timers SV4 drops-out and deasserts SEL variable SV5 and line breaker trip output (OUT101).	SV4T SV5 OUT101
13	11.0	SEL variable/timer SV3 drops-out and deasserts OUT103 to return the line breaker trip contact to the trip coil circuit.	SV3T OUT103
14	11.0 +	Deassert OUT104 to reconnect the line breaker trip contacts to the trip coils.	OUT104

Self-Testing and Monitoring

The 21S contains self checking logic to exercise the microprocessor. It also monitors the voltage applied to the relay and generates a loss of potential (LOP) alarm if one or more of the voltages are out of range. The self-check alarm is alarmed through the ALARM output and all of the other failure alarms are alarmed through OUT107 as follows:

1. Loss of potential (LOP)
2. Line breaker trip coil monitor fail (SV1T and LT1)
3. Line breaker trip output contact test fail (SV7 and LT1)

Items 2 and 3 operate alarm latch LT1 and can only be reset by pulsing remote bit RB04. This is designed to require a qualified person to access the relay, either locally or remotely, to determine the cause of the failure and appropriate action.

Oscillographic Fault Recording

The 21S relay automatically captures an oscillographic record of the currents, voltages and internal relay data for all trips initiated from the secondary relay.

Sequence Of Events Recording

The time stamped status of selected discrete data in the secondary relay is written to the sequence of events record. This is a first-in-first-out list of the most recent 500 status change events.