called the bus impedance matrix $\mathbf{Z}_{\text{bus}}$. Performing the indicated matrix multiplication yields

$$\begin{bmatrix} 1.4111 - j0.2668 \\ 1.3830 - j0.3508 \\ 1.4059 - j0.2824 \\ 1.4009 - j0.2971 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}$$

and so the node voltages are

$$V_1 = 1.4111 - j0.2668 = 1.436 \underline{/-10.71^\circ} \text{ per unit}$$

$$V_2 = 1.3830 - j0.3508 = 1.427 \underline{/-14.24^\circ} \text{ per unit}$$

$$V_3 = 1.4059 - j0.2824 = 1.434 \underline{/-11.36^\circ} \text{ per unit}$$

$$V_4 = 1.4009 - j0.2971 = 1.432 \underline{/-11.97^\circ} \text{ per unit}$$

END
LECTURE
NO. 20

7.3 MATRIX PARTITIONING

A useful method of matrix manipulation, called *partitioning*, consists in recognizing various parts of a matrix as submatrices which are treated as single elements in applying the usual rules of multiplication and addition. For instance, assume a 3 × 3 matrix **A**, where

$$\mathbf{A} = \left[\begin{array}{cc:c} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ \hdashline a_{31} & a_{32} & a_{33} \end{array}\right] \tag{7.11}$$

The matrix is partitioned into four submatrices by the horizontal and vertical dashed lines. The matrix may be written

$$\mathbf{A} = \begin{bmatrix} \mathbf{D} & \mathbf{E} \\ \mathbf{F} & \mathbf{G} \end{bmatrix} \tag{7.12}$$

where the submatrices are

$$\mathbf{D} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \qquad \mathbf{E} = \begin{bmatrix} a_{13} \\ a_{23} \end{bmatrix}$$

$$\mathbf{F} = [a_{31} \quad a_{32}] \qquad \mathbf{G} = a_{33}$$

To show the steps in matrix multiplication in terms of submatrices let us assume that **A** is to be postmultiplied by another matrix **B** to form the product **C**, where

$$\mathbf{B} = \left[\begin{array}{c} b_{11} \\ b_{21} \\ \hdashline b_{31} \end{array}\right] \tag{7.13}$$

With partitioning as indicated,

$$\mathbf{B} = \begin{bmatrix} \mathbf{H} \\ \mathbf{J} \end{bmatrix} \tag{7.14}$$

where the submatrices are

$$\mathbf{H} = \begin{bmatrix} b_{11} \\ b_{21} \end{bmatrix} \qquad \text{and} \qquad \mathbf{J} = b_{31}$$

Then the product is

$$\mathbf{C} = \mathbf{AB} = \begin{bmatrix} \mathbf{D} & \mathbf{E} \\ \mathbf{F} & \mathbf{G} \end{bmatrix} \begin{bmatrix} \mathbf{H} \\ \mathbf{J} \end{bmatrix} \tag{7.15}$$

The submatrices are treated as single elements to obtain

$$\mathbf{C} = \begin{bmatrix} \mathbf{DH} + \mathbf{EJ} \\ \mathbf{FH} + \mathbf{GJ} \end{bmatrix} \tag{7.16}$$

The product is finally determined by performing the indicated multiplication and addition of the submatrices.

If **C** is composed of the submatrices **M** and **N** so that

$$\mathbf{C} = \begin{bmatrix} \mathbf{M} \\ \mathbf{N} \end{bmatrix} \tag{7.17}$$

comparison with Eq. (7.16) shows

$$\mathbf{M} = \mathbf{DH} + \mathbf{EJ} \tag{7.18}$$

$$\mathbf{N} = \mathbf{FH} + \mathbf{GJ} \tag{7.19}$$

If we wish to find only the submatrix **N**, partitioning shows that

$$\begin{aligned} \text{N} &= [a_{31} \quad a_{32}] \begin{bmatrix} b_{11} \\ b_{21} \end{bmatrix} + a_{33}b_{31} \\ &= a_{31}b_{11} + a_{32}b_{21} + a_{33}b_{31} \end{aligned} \tag{7.20}$$

The matrices to be multiplied must be compatible originally. Each vertical partitioning line between columns r and $r + 1$ of the first factor requires a horizontal partitioning line between rows r and $r + 1$ of the second factor in order for the submatrices to be multiplied. Horizontal partitioning lines may be drawn between any rows of the first factor, and vertical lines between any columns of the second, or omitted in either or both. An example that applies matrix partitioning appears at the end of the next section.

7.4 NODE ELIMINATION BY MATRIX ALGEBRA

Nodes may be eliminated by matrix manipulation of the standard node equations. However, only those nodes at which current does not enter or leave the network can be eliminated.

The standard node equations in matrix notation are expressed as

$$\mathbf{I} = \mathbf{Y}_{\text{bus}}\mathbf{V} \tag{7.21}$$

where **I** and **V** are column matrices and $\mathbf{Y}_{\text{bus}}$ is a symmetrical square matrix. The column matrices must be so arranged that elements associated with nodes to be eliminated are in the lower rows of the matrices. Elements of the square admittance matrix are located correspondingly. The column matrices are partitioned so that the elements associated with nodes to be eliminated are separated from the other elements. The admittance matrix is partitioned so that elements identified only with nodes to be eliminated are separated from the other elements by horizontal and vertical lines. When partitioned according to these rules, Eq. (7.21) becomes

$$\begin{bmatrix}\mathbf{I}_A\\ \mathbf{I}_X\end{bmatrix} = \begin{bmatrix}\mathbf{K} & \mathbf{L}\\ \mathbf{L}^T & \mathbf{M}\end{bmatrix}\begin{bmatrix}\mathbf{V}_A\\ \mathbf{V}_X\end{bmatrix} \tag{7.22}$$

where $\mathbf{I}_X$ is the submatrix composed of the currents entering the nodes to be eliminated and $\mathbf{V}_X$ is the submatrix composed of the voltages of these nodes. Of course, every element in $\mathbf{I}_X$ is zero, for the nodes could not be eliminated otherwise. The self- and mutual admittances composing **K** are those identified only with nodes to be retained. **M** is composed of the self- and mutual admittances identified only with nodes to be eliminated. It is a square matrix whose order is equal to the number of nodes to be eliminated. **L** and its transpose $\mathbf{L}^T$ are composed of only those mutual admittances common to a node to be retained and to one to be eliminated.

Performing the multiplication indicated in Eq. (7.22) gives

$$\mathbf{I}_A = \mathbf{K}\mathbf{V}_A + \mathbf{L}\mathbf{V}_X \tag{7.23}$$

and

$$\mathbf{I}_X = \mathbf{L}^T\mathbf{V}_A + \mathbf{M}\mathbf{V}_X \tag{7.24}$$

Since all elements of $\mathbf{I}_X$ are zero, subtracting $\mathbf{L}^T\mathbf{V}_A$ from both sides of Eq. (7.24) and multiplying both sides by the inverse of **M** (denoted by $\mathbf{M}^{-1}$) yields

$$-\mathbf{M}^{-1}\mathbf{L}^T\mathbf{V}_A = \mathbf{V}_X \tag{7.25}$$

This expression for $\mathbf{V}_X$ substituted in Eq. (7.23) gives

$$\mathbf{I}_A = \mathbf{K}\mathbf{V}_A - \mathbf{L}\mathbf{M}^{-1}\mathbf{L}^T\mathbf{V}_A \tag{7.26}$$

which is a node equation having the admittance matrix

$$\mathbf{Y}_{\text{bus}} = \mathbf{K} - \mathbf{L}\mathbf{M}^{-1}\mathbf{L}^T \tag{7.27}$$

This admittance matrix enables us to construct the circuit with the unwanted nodes eliminated, as we shall see in the following example.

Example 7.3 If the generator and transformer at bus 3 are removed from the circuit of Fig. 7.3, eliminate nodes 3 and 4 by the matrix-algebra procedure just described, find the equivalent circuit with these nodes eliminated, and find the complex power transferred into or out of the network at nodes 1 and 2. Also find the voltage at node 1.

SOLUTION The bus admittance matrix of the circuit partitioned for elimination of nodes 3 and 4 is

$$\mathbf{Y}_{\text{bus}} = \begin{bmatrix}\mathbf{K} & \mathbf{L}\\ \mathbf{L}^T & \mathbf{M}\end{bmatrix} = \left[\begin{array}{cc:cc} -j9.8 & 0.0 & j4.0 & j5.0\\ 0.0 & -j8.3 & j2.5 & j5.0\\ \hdashline j4.0 & j2.5 & -j14.5 & j8.0\\ j5.0 & j5.0 & j8.0 & -j18.0 \end{array}\right]$$

The inverse of the submatrix in the lower right position is

$$\mathbf{M}^{-1} = \frac{1}{-197}\begin{bmatrix}-j18.0 & -j8.0\\ -j8.0 & -j14.5\end{bmatrix} = \begin{bmatrix}j0.0914 & j0.0406\\ j0.0406 & j0.0736\end{bmatrix}$$

Then

$$\mathbf{L}\mathbf{M}^{-1}\mathbf{L}^T = \begin{bmatrix}j4.0 & j5.0\\ j2.5 & j5.0\end{bmatrix}\begin{bmatrix}j0.0914 & j0.0406\\ j0.0406 & j0.0736\end{bmatrix}\begin{bmatrix}j4.0 & j2.5\\ j5.0 & j5.0\end{bmatrix}$$

$$= -\begin{bmatrix}j4.9264 & j4.0736\\ j4.0736 & j3.4264\end{bmatrix}$$

$$\mathbf{Y}_{\text{bus}} = \mathbf{K} - \mathbf{L}\mathbf{M}^{-1}\mathbf{L}^T = \begin{bmatrix}-j9.8 & 0.0\\ 0.0 & -j8.3\end{bmatrix} - \mathbf{L}\mathbf{M}^{-1}\mathbf{L}^T$$

$$\mathbf{Y}_{\text{bus}} = \begin{bmatrix}-j4.8736 & j4.0736\\ j4.0736 & -j4.8736\end{bmatrix}$$

Examination of the matrix shows us that the admittance between the two remaining buses 1 and 2 is $-j4.0736$, the reciprocal of which is the per-impedance between these buses. The admittance between each of these b and the reference bus is

$$-j4.8736 - (-j4.0736) = -j0.800 \text{ per unit}$$

The resulting circuit is shown in Fig. 7.5*a*. When the current sources converted to their equivalent emf sources the circuit, with impedances in unit, is that of Fig. 7.5*b*. Then the current is

$$I = \frac{1.5\underline{/0^\circ} - 1.5\underline{/-36.87^\circ}}{j(1.25 + 1.25 + 0.2455)} = \frac{1.5 - 1.2 + j0.9}{j(2.7455)}$$

$$= 0.3278 - j0.1093 = 0.3455\underline{/-18.44} \text{ per unit}$$

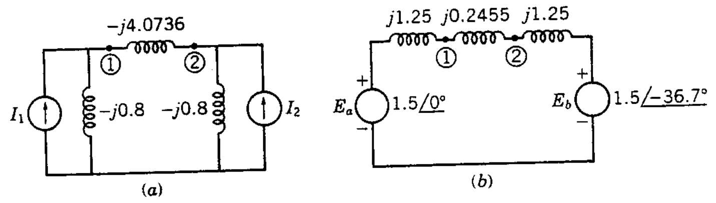

Figure 7.5 Circuit of Fig. 7.3 without the source at node 3 (*a*) with the equivalent current sources and (*b*) with the original voltage sources at nodes 1 and 2.

Power *out* of source *a* is

$$1.5\underline{/0^\circ} \times 0.3455\underline{/18.44^\circ} = 0.492 + j0.164 \text{ per unit}$$

And power *into* source *b* is

$$1.5\underline{/-36.87^\circ} \times 0.3455\underline{/18.44^\circ} = 0.492 - j0.164 \text{ per unit}$$

Note that the reactive voltamperes in the circuit equal

$$(0.3455)^2 \times 2.7455 = 0.328 = 0.164 + 0.164$$

The voltage at node 1 is

$$1.50 - j1.25(0.3278 - j0.1093) = 1.363 - j0.410 \text{ per unit}$$

In the simple circuit of this example node elimination could have been accomplished by Y-Δ transformations and by working with series and parallel combinations of impedances. The matrix partitioning method is a general method which is thereby more suitable for computer solutions. However, for the elimination of a large number of nodes, the matrix **M** whose inverse must be found will be large.

Inverting a matrix is avoided by eliminating one node at a time, and the process is very simple. The node to be eliminated must be the highest numbered node, and renumbering may be required. The matrix **M** becomes a single element and $\mathbf{M}^{-1}$ is the reciprocal of the element. The original admittance matrix partitioned into submatrices **K**, **L**, $\mathbf{L}^T$, and **M** is

$$\mathbf{Y}_{\text{bus}} = \left[\begin{array}{ccccc:c} \overbrace{Y_{11} & \cdots & Y_{1j} & \cdots}^{\mathbf{K}} & & Y_{1n} \\ \vdots & & \vdots & & & \vdots \\ Y_{k1} & \cdots & Y_{kj} & \cdots & & Y_{kn} \\ \vdots & & \vdots & & & \vdots \\ \hdashline \underbrace{Y_{n1} & \cdots & Y_{nj} & \cdots}_{\mathbf{L}^T} & & \underbrace{Y_{nn}}_{\mathbf{M}} \end{array}\right] \Big\} \mathbf{L} \qquad (7.28)$$

the reduced $(n-1) \times (n-1)$ matrix will be, according to Eq. (7.27),

$$\mathbf{Y}_{\text{bus}} = \begin{bmatrix} Y_{11} & \cdots & Y_{1j} & \cdots \\ \vdots & & \vdots & \\ Y_{k1} & \cdots & Y_{kj} & \cdots \\ \vdots & & \vdots & \end{bmatrix} - \frac{1}{Y_{nn}} \begin{bmatrix} Y_{1n} \\ \vdots \\ Y_{kn} \\ \vdots \end{bmatrix} [Y_{n1} \cdots Y_{nj} \cdots] \qquad (7.29)$$

and when the indicated manipulation of the matrices is accomplished, the element in row k and column j of the resulting $(n-1) \times (n-1)$ matrix will be

$$Y_{kj\,(\text{new})} = Y_{kj\,(\text{orig})} - \frac{Y_{kn} Y_{nj}}{Y_{nn}} \qquad (7.30)$$

Each element in the original matrix **K** must be modified. When Eq. (7.28) is compared to Eq. (7.30) we can see how to proceed. We multiply the element in the last column and the same row as the element being modified by the element in the last row and the same column as the element being modified. We then divide this product by Y_{nn} and subtract the result from the element being modified. The following example illustrates the simple procedure.

Example 7.4 Perform the node elimination of Example 7.3 by first removing node 4 and then by removing node 3.

Solution As in Example 7.3, the original matrix now partitioned for removal of one node is

$$\mathbf{Y}_{\text{bus}} = \left[\begin{array}{ccc:c} -j9.8 & 0.0 & j4.0 & j5.0 \\ 0.0 & -j8.3 & j2.5 & j5.0 \\ j4.0 & \enclose{circle}{j2.5} & -j14.5 & \boxed{j8.0} \\ \hdashline j5.0 & \boxed{j5.0} & j8.0 & -j18.0 \end{array}\right]$$

To modify the element $j2.5$ in row 3, column 2 subtract from it the product of the elements enclosed by rectangles and divided by the element in the lower right corner. We find the modified element

$$Y_{32} = j2.5 - \frac{j8.0 \times j5.0}{-j18.0} = j4.7222$$

Similarly the new element in row 1, column 1 is

$$Y_{11} = -j9.8 - \frac{j5.0 \times j5.0}{-j18.0} = -j8.4111$$

Other elements are found in the same manner to yield

$$\mathbf{Y}_{\text{bus}} = \begin{bmatrix} -j8.4111 & j1.3889 & j6.2222 \\ j1.3889 & -j6.9111 & j4.7222 \\ j6.2222 & j4.7222 & -j10.9444 \end{bmatrix}$$

Reducing the above matrix to remove node 3 yields

$$\mathbf{Y}_{\text{bus}} = \begin{bmatrix} -j4.8736 & j4.0736 \\ j4.0736 & -j4.8736 \end{bmatrix}$$

which is identical to the matrix found by the matrix-partitioning method where two nodes were removed at the same time.

D
CTURE 23

7.5 THE BUS ADMITTANCE AND IMPEDANCE MATRICES

In Example 7.2, we inverted the bus admittance matrix $\mathbf{Y}_{\text{bus}}$ and called the resultant matrix the bus impedance matrix $\mathbf{Z}_{\text{bus}}$. By definition

$$\mathbf{Z}_{\text{bus}} = \mathbf{Y}_{\text{bus}}^{-1} \tag{7.31}$$

and for a network of three independent nodes

$$\mathbf{Z}_{\text{bus}} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \tag{7.32}$$

Since $\mathbf{Y}_{\text{bus}}$ is symmetrical around the principal diagonal, $\mathbf{Z}_{\text{bus}}$ must be symmetrical in the same manner.

The impedance elements of $\mathbf{Z}_{\text{bus}}$ on the principal diagonal are called *driving-point impedance of the nodes*, and the off-diagonal elements are called the *transfer impedances of the nodes*.

The bus admittance matrix need not be determined in order to obtain $\mathbf{Z}_{\text{bus}}$, and in another section of this chapter we shall see how $\mathbf{Z}_{\text{bus}}$ may be formulated directly.

The bus impedance matrix is important and very useful in making fault calculations as we shall see later. In order to understand the physical significance of the various impedances in the matrix we shall compare them with the node admittances. We can easily do so by looking at the equations at a particular node. For instance, starting with the node equations expressed as

$$\mathbf{I} = \mathbf{Y}_{\text{bus}}\mathbf{V} \tag{7.33}$$

we have at node 2 of the three independent nodes

$$I_2 = Y_{21}V_1 + Y_{22}V_2 + Y_{23}V_3 \tag{7.34}$$

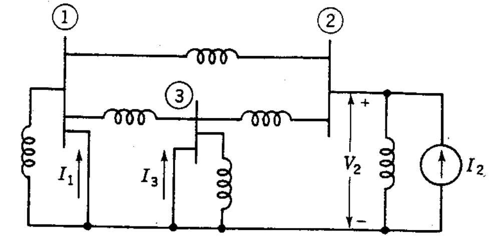

Figure 7.6 Circuit for measuring Y_{22}, Y_{12}, and Y_{32}.

If V_1 and V_3 are reduced to zero by shorting nodes 1 and 3 to the reference node and current I_2 is injected at node 2, the self-admittance at node 2 is

$$Y_{22} = \frac{I_2}{V_2}\bigg|_{V_1=V_3=0} \tag{7.35}$$

Thus, the self-admittance of a particular node could be measured by shorting all other nodes to the reference node and then finding the ratio of the current injected at the node to the voltage resulting at that node. Figure 7.6 illustrates the method for a three-node reactive network. The result is obviously equivalent to adding all the admittances directly connected to the node, as has been our procedure up to now.

Figure 7.6 also serves to illustrate mutual admittance. At node 1 the equation obtained by expanding Eq. (7.33) is

$$I_1 = Y_{11}V_1 + Y_{12}V_2 + Y_{13}V_3 \tag{7.36}$$

from which we see that

$$Y_{12} = \frac{I_1}{V_2}\bigg|_{V_1=V_3=0} \tag{7.37}$$

Thus the mutual admittance is measured by shorting all nodes except node 2 to the reference node and injecting a current I_2 at node 2, as shown in Fig. 7.6. Then Y_{12} is the ratio of the negative of the current leaving the network in the short circuit at node 1 to the voltage V_2. The negative of the current *leaving* node 1 is used since I_1 is defined as the current *entering* the network. The resultant admittance is the negative of the admittance directly connected beween nodes 1 and 2, as we would expect.

We have made this detailed examination of the node admittances in order to differentiate them clearly from the impedances of the bus impedance matrix.

We solve Eq. (7.33) by premultiplying both sides of the equation by $\mathbf{Y}_{\text{bus}}^{-1} = \mathbf{Z}_{\text{bus}}$ to yield

$$\mathbf{V} = \mathbf{Z}_{\text{bus}}\mathbf{I} \tag{7.38}$$

and we must remember when dealing with $\mathbf{Z}_{\text{bus}}$ that $\mathbf{V}$ and $\mathbf{I}$ are column matrices of the node voltages and the currents entering the nodes from current sources,