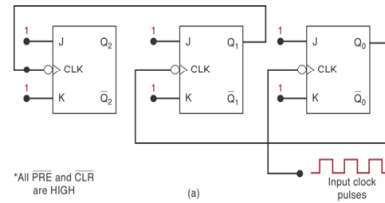


Example 5 - 14

- If the circuit of 3-bit counter is changed to have 6 FFs:
 - Determine the counter's MOD number
 - MOD number = $2^6 = 64$
 - Determine the Frequency of the last FFs (Q5) when the input frequency is 1 MHz
 - $f = 1\text{MHz}/64 = 15.625\text{ kHz}$
 - What is the range of counting states for this counter?
 - 000000 to 111111 (0 to 63), number of states = 64
 - Assume a starting state (000000). What will be the counter's state after 129 pulses?
 - Counter will be back to its starting state every 64 pulses. So the 129th Pulse will bring the counter to state (000001)

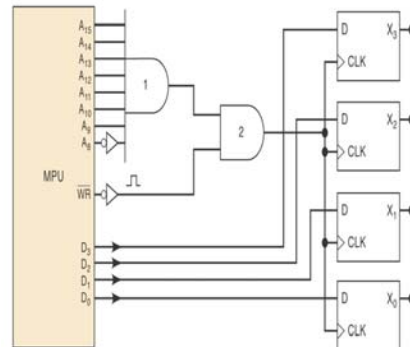


Slide - 198

EET2411
DIGITAL ELECTRONICS

Example 5 - 15

- What address code must MPU generate in order for the data to be transferred into X?
 - $(A_{15}..A_8) = (11111110)$
- Assume that $X_3-X_0 = 0110$, $A_{15}-A_8 = 11111111$, $D_3-D_0 = 1011$. What will be the contents of X after WR* pulse occurs?
 - Since $A_8 = 1$, X register will not be addressed and the content will not change (0110)



Slide - 200

EET2411
DIGITAL ELECTRONICS

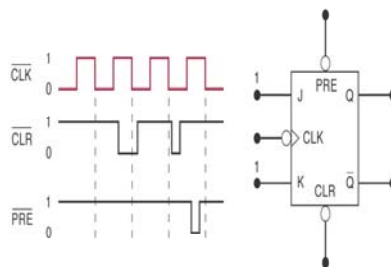
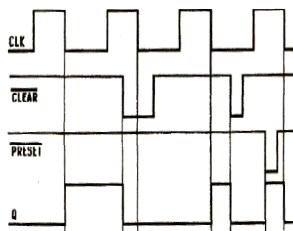
Midterm II Review - Topics

- **Digital Arithmetic (Chapter 6)**
 - Binary addition, signed numbers representation, 2's complement, Subtraction in 2's complement, overflow
 - Multiplication/Division of binary numbers
 - Arithmetic circuits (ALU), parallel binary adder, Design of a Full Adder
 - ALU integrated circuits (74382)
- **Flip-Flops & Related Devices (Chapter 5)**
 - NAND/NOR Latch
 - Clocked FF (SC, JK, D)
 - FFs timing consideration
 - Setup/hold time.
 - FFs Application
 - Parallel/Serial Data Transfer
 - Frequency Divider/Counting
 - Asynchronous counter
 - MOD number
 - State Transition Diagram

Problem - 1

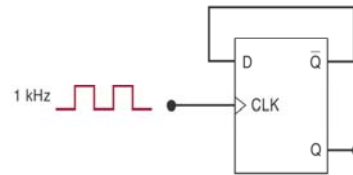
- Determine the Q waveform for the J-K FF. Assume that $Q = 0$ initially. (Hint: the asynchronous inputs override all other inputs) :

J=K=1 so FF will toggle on each CLK negative-going edge, unless either $\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ inputs is LOW.



Problem 2

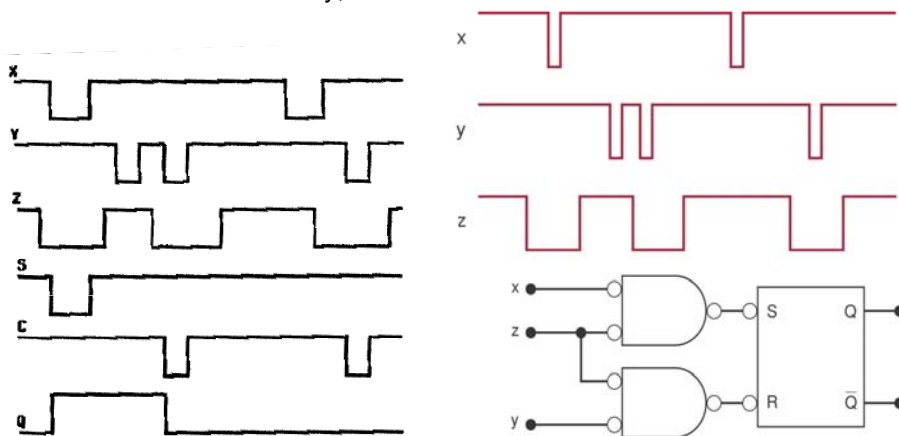
- An edge-triggered D flip-flop can be made to operate in the toggle mode by connecting it as shown.
 - Assume that $Q = 0$ initially, determine the Q waveform
 - Change the circuit so that Q is connected back to D , then determine the Q waveform.



- If Q initially = 0, then Q is $\frac{1}{2}$ frequency of the clock, 500 Hz
- If Q is connected to D , then Q will not change as clock applied.

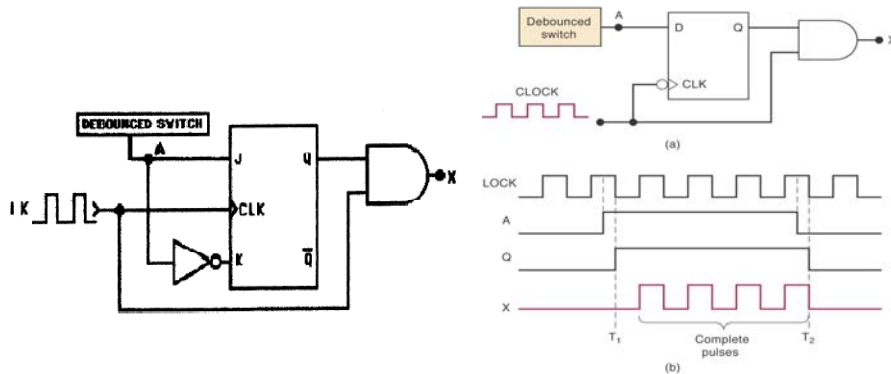
Problem 3

- Assume $Q = 0$ initially, determine the Q waveform.



Problem 4

- Modify the circuit to use a JK FF instead.

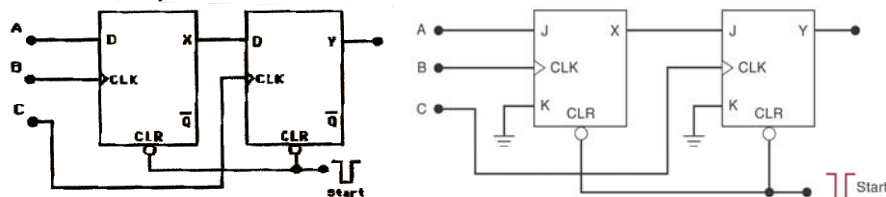


EET2411
DIGITAL ELECTRONICS

Slide - 209

Problem - 5

- The following circuit has inputs A, B, and C all initially LOW. Output Y is supposed to go HIGH only when A, B, and C go HIGH in a certain sequence.
 - Determine the sequence that will make Y go HIGH.
 - Explain why the start pulse is needed.
 - Modify the circuit to use D FFs.



- Y will go High if C goes high while X is High. X can go High only if B goes High while A is High, the correct sequence A, B, C.
- The Start pulse is used to clear the FF X, Y before applying the ABC signals.

EET2411
DIGITAL ELECTRONICS

Slide - 211