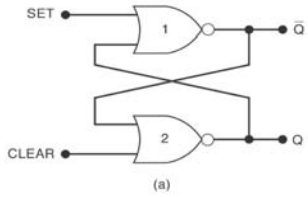
5-2 NOR Gate Latch

- The NOR latch is similar to the NAND latch except that the Q and $\overline{Q}$ outputs are reversed.
- The set and clear inputs are active high, that is, the output will change when the input is pulsed high.
- In order to ensure that a FF begins operation at a known level, a pulse may be applied to the set or clear inputs when a device is powered up.

NOR gate latch: truth table and simplified block symbol

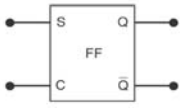


(a)

Set	Clear	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

*Produces Q = Q̄ = 0.

(b)

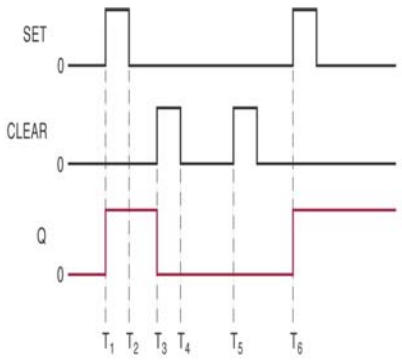


(c)

- Summary of the NAND latch:
  - Set = clear = 0. Normal resting state, outputs remain in state prior to input.
  - Set = 1, clear = 0. Q will go high and remain high even if the set input goes low.
  - Set = 0, clear = 1. Q will go low and remain low even if the clear input goes low.
  - Set = clear = 1. Output is unpredictable because the latch is being set and cleared at the same time.

Example 5-3

- Waveforms are applied at the NOR latch:
  - Assume that initially Q=0, determine the Q waveform.
    - SET=CLEAR=0, no change
    - At T1, high pulse on SET causes Q to go high and remain high
    - At T2, low pulse on SET will cause no effect on Q.
    - At T3, high pulse on CLEAR will clear Q, Q=0 and remains low even after CLEAR return low at T4.
    - At T5, high pulse on CLEAR will have no effect on Q
    - St T6, a high pulse on SET causes Q to go back High and stays high



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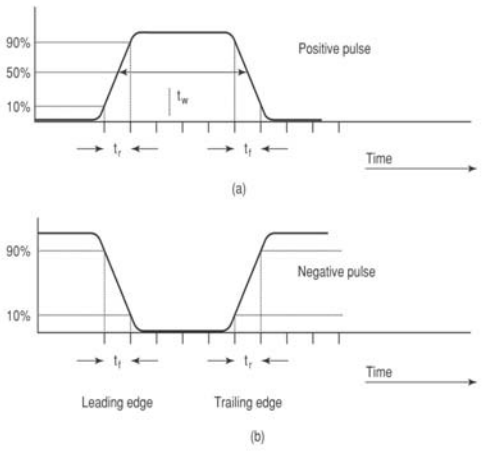
5-4 Digital Pulses

- Signals that switch between active and inactive states are called pulse waveforms.
  - A positive pulse has an active high level.
  - A negative pulse has an active low level.



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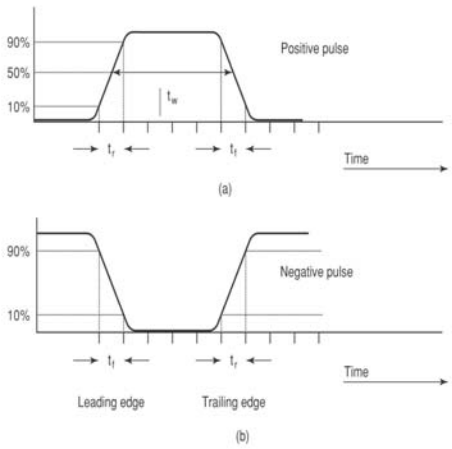
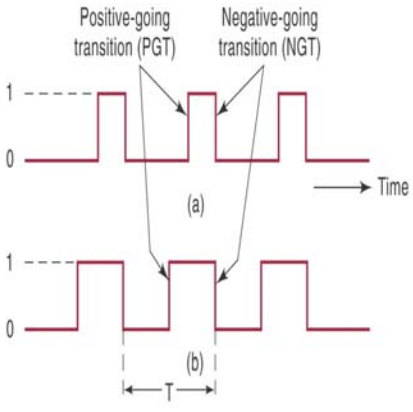
5-4 Digital Pulses

- The transition from low to high on a positive pulse is called rise time (t_r).
  - Rise time is measured between the 10% and 90% points on the leading edge of the voltage waveform.
- The transition from high to low on a positive pulse is called fall time (t_f).
  - Fall time is measured between the 90% and 10% points on the trailing edge of the voltage waveform.
- The pulse width (t_w) is defined as the time between the points when the leading and trailing edges are at 50% of the high level.



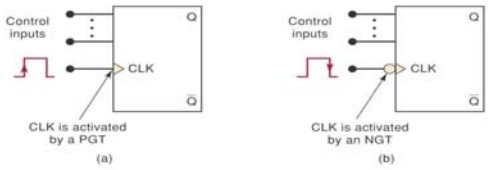
5-5 Clock Signals and Clocked Flip-Flops

- Asynchronous system – outputs can change state at any time the input(s) change. Difficult to design and debug.
- Synchronous system – output can change state only at a specific time in the clock cycle.
  - The clock signal is a rectangular pulse train or square wave. It is distributed to all parts of the system.
  - Positive going transition (PGT) – when clock pulse goes from 0 to 1.
  - Negative going transition (NGT) – when clock pulse goes from 1 to 0.
  - Transitions are also called edges.
  - Most digital systems are principally synchronous.
  - The speed of the synchronous system depends on clock speed.
  - A clock period is measured between PGT to the next PGT, seconds/cycle (T).
  - The speed of the system is normally referred as number of cycles in 1 second, Frequency of the clock, (Hertz = 1 cycle/second).



5-5 Clock Signals and Clocked Flip-Flops

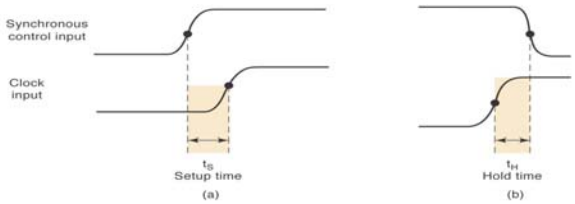
- Clocked FFs change state on one or the other clock transitions. Some common characteristics:
  - Clock inputs are labeled CLK, CK, or CP mainly edge-triggered.
  - A small triangle at the CLK input indicates that the input is activated with a PGT.
  - A bubble and a triangle indicates that the CLK input is activated with a NGT.
  - Control inputs have an effect on the output only at the active clock transition (NGT or PGT). These are also called synchronous control inputs.
  - The control inputs get the FF outputs ready to change (determine What), but the change is not triggered until the CLK edge (determine when).



5-5 Clock Signals and Clocked Flip-Flops

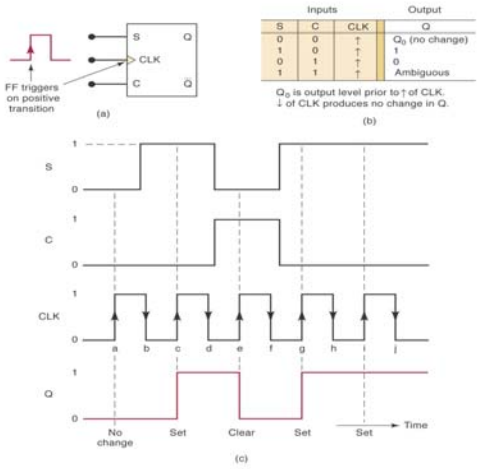
- Setup time, t_S is the minimum time interval before the active CLK transition that the control input must be kept at the proper level.
- Hold time, t_H is the time following the active transition of the CLK during which the control input must kept at the proper level.

The control inputs must be stable for at least t_S(min) prior the clk transition & at least t_H(min) after the clk transition



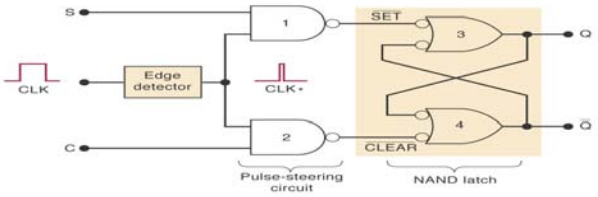
5-6 Clocked S-C Flip-Flop

- The set-clear (or set-reset) FF will change states at the positive going or negative going clock edge.
- FF is only affected by PGT transition at points (a, c, e, g, i)

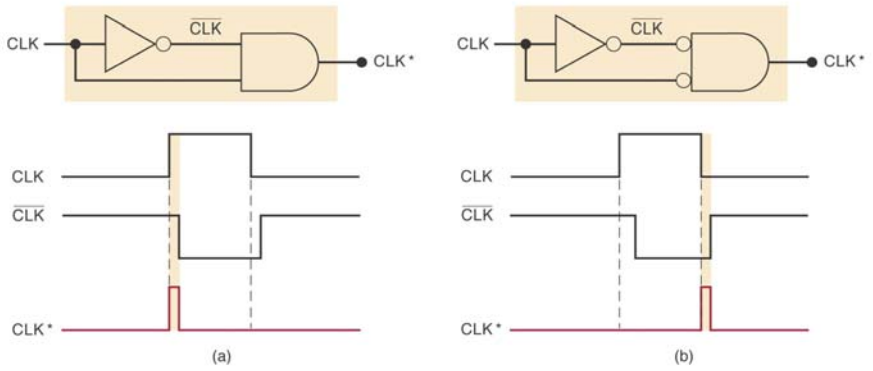


internal circuitry for an edge-triggered S-C flip-flop

- Basic NAND gate latch formed by NAND(3,4)
- Pulse-steering circuit formed by NAND(1,2)
- Edge-detector circuit
- Edge detector produces a narrow positive going spike (CLK*) that coincident with the PGT of the CLK
- The pulse circuits steers the spike through to the SET or CLEAR input in accordance with the level present on S and C
- When S=1, C=0, the CLK* produces a low pulse at the SET input of the latch.



Implementation of edge-detector circuits used in edge-triggered flip-flops: (a) PGT; (b) NGT.



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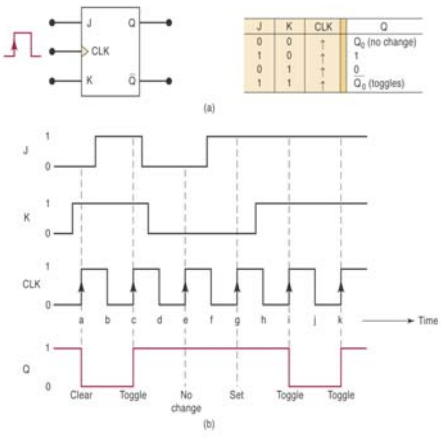
5-7 Clocked J-K Flip-Flop

- Operates like the S-C FF. J is set, K is clear.
- When J and K are both high the output is toggled from whatever state it is in to the opposite state.
- May be positive going or negative going clock trigger.
- Has the ability to do everything the S-C FF does, plus operate in toggle mode.



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internal circuitry for an edge-triggered J-K flip-flop

- Same as edge-triggered S-C flip-flop
- The only difference is that the Q, $\overline{Q}$ outputs are fed back to the pulse-steering NAND gate, this causes J-K to toggle for J=K=1
- Assume J=K=1 and Q is low, NAND gate 1 steers CLK* to $\overline{SET}$ of the NAND latch to produce Q = 1.
- The opposite will occur if we starts with Q=1