EET2142 - DIGITAL DESIGN & MODELING USING VHDL
3 CREDITS - SPRING 2012

Course Description: The course emphasizes on the language concepts of digital systems design using VHSIC Hardware Description Language with an emphasis on good digital design practices, and writing testbenches for design verification. Students will gain valuable hands-on experience on writing efficient hardware designs using VHDL and perform high-level HDL simulations using ModelSim

Instructor: Dr. Nasser Alaraje
Room 417 EERC Bldg.
Phone: 487-1661
E-mail: alaraje@mtu.edu

Office Hours: MW 1:00 – 3:00 pm, (or by appointment)

Prerequisite: EET2141

Classroom/Time:	R01	MW	10:05 am-10:55 am – EERC313
Lab/Time:	L01	R	01:05 pm-02:55 pm, EERC421

Course Webpage: http://www.tech.mtu.edu/~alaraje/Spring2012/EET2142/EET2142Spring2012.html

Text Book: VHDL: Astarter's Guide (2nd ed.), Sudhakar Yalamanchili, Prentice-Hall, 2005.

References: Digital Systems: Principles and Applications by R. J. Tocci and N. S. Widmer, the 10th edition, Prentice Hall, 2007
VHDL For Digital Design, 1st edition, Frank Vahid, Wiley, 2007

Course Objectives:

- To be able to model basic digital circuits in hardware description languages
- To be able to use VHDL to model common digital hardware circuits
- To be able to use VHDL CAD Tools (editors, debug designs and perform logic simulation)
- To be able write test benches to verify the design and perform timing analysis of a given design.
- To gain the knowledge on programmable logic devices (PLD) and their design methodologies and know about different design entry methods

Topics:

- Digital Logic Design Fundamentals
- Design Flow Methodology
- VHDL - What is it and Why ?
- Language Fundamentals (Entity, Architecture, Sequential and Concurrent Statements, Configuration)
- Test benches
- Sequential Statements (IF, FOR LOOP, CASE, FOR GENERATE, Assertion/Report)
- Concurrent Statements
- Modeling Latches, Flip-flops, Multiplexers, Address decoder, Shift register, Counters

- Description of a Register Bank
- Procedure-based test bench
- Scalar data types and Operations
- Composite Data types and Operations
- Arrays - Constrained, Unconstrained, constant and array mappings
- Packages
- Resolved Signals
- Generics
- Shared variables
- State Machines (Definition, types, examples and Industry rules)
- Coding Tips and techniques for synthesizable, reusable VHDL
- Coding Tips for creating synthesizable, reusable VHDL
- How to synthesize a design?

Grading:

Your final grade is based on the grade weighting plan below which gives you the highest grade, 70% of your grade toward class as follows:

	Plan A	Plan B	
Lab Assignments	30%	30%	
Homework, Quizzes,Term Project	10%	10%	
Hour exams	40%	20%	**Week 5 and Week 10**
Final exam	20%	40%	

Scale:

90-100	A	70-74	C
85-89	AB	65-69	CD
80-84	B	60-64	D
75-79	BC	0 -59	F

Computer Usage: *Altera* Quartus® II software version 9.1
Mentor Graphics ModelSim Software SE 6.5b

Cheating: University rules require that any student caught cheating or copying from another student receive a failing grade for the course and be reported to the Dean of Students. **Copying includes copying or sharing any part of a computer file.**

Make-up policy:

- The final examination may only be taken at the scheduled time. You *must not* make travel plans that conflict with the final exam schedule.
- Midterm examinations may be made up only due to illness on the day of the exam (a doctor's note is required) or by advance arrangement (a written request one week in advance of the exam is required). The instructor reserves the right to deny any advance request for a make-up exam.

Use of Electronic Devices:

Cell phones, Blackberries, iPods, PDAs, or any other electronic devises **are not to be used in the classroom**. Please make sure to bring a calculator with you to class. Calculators on other devices are strictly prohibited. Information exchanges on these devices during class are also prohibited and violate the Academic Integrity Code of Michigan Tech.

University Policies:

Academic regulations and procedures are governed by University policy. Academic dishonesty cases will be handled in accordance the University's policies. If you have a disability that could affect your performance in this class or that requires an accommodation under the Americans with Disabilities Act, please see me as soon as possible so that we can make appropriate arrangements. The Affirmative Action Office has asked that you be made aware of the following:

Michigan Tech complies with all federal and state laws and regulations regarding discrimination, including the Americans with Disabilities Act of 1990. If you have a disability and need a reasonable accommodation for equal access to education or services at Michigan Tech, please call the Dean of Students Office, at 487-2212. For other concerns about discrimination, you may contact your advisor, department head or the Affirmative Action Office, at 487-3310

Academic Integrity: http://www.studentaffairs.mtu.edu/dean/judicial/policies/academic_integrity.html
Affirmative Action: http://www.admin.mtu.edu/aao/
Disability Services: http://www.admin.mtu.edu/urel/studenthandbook/student_services.html#disability

Changes:

This syllabus is subject to change as found appropriated by the instructor. The changes will be announced in class in a timely fashion.