EE5780 Advanced VLSI CAD

Lecture 1 Introduction
Zhuo Feng
Prof. Zhuo Feng
▶ Office:  EERC 513
▶ Phone:  487-3116
▶ Email:  zhuofeng@mtu.edu

Class Website
▶ http://www.ece.mtu.edu/~zhuofeng/EE5780Fall2013.html
▶ Check the class website for lecture materials, assignments and announcements

Schedule
▶ TR 11:05pm-12:20pm EERC 508
▶ Office hours: TR 4:00pm – 5:00pm or by appointments
Topics (tentative)

1. Introduction
2. CMOS circuit and layout
3. MOS transistor device characteristics
4. DC and transient responses, delay estimation
5. Logical effort
6. Power estimation and reduction
7. Modified nodal analysis and SPICE simulation
8. Interconnect modeling and analysis
9. Combinational circuits design and modeling
10. Sequential circuits
11. Statistical timing analysis
12. SRAM design and yield analysis
13. Power & clock distribution networks design, modeling and analysis
Grading Policy

- Homework: 30%
- Mid-term Exam: 30%
- Final Exam: 30%
- Class Attendance: 10%
- Letter Grades:
  - A: 85~100; AB: 80~84; B: 75~79; BC: 70~74; C: 65~69; D: 60~64; F: 0~59
Moore’s law in Microprocessors

Transistors on Lead Microprocessors double every 2 years

Courtesy, Intel
Die Size Growth

Die size grows by 14% to satisfy Moore’s Law

Courtesty, Intel
Frequency

Doubles every 2 years

Lead Microprocessors frequency doubles every 2 years

Courtesy, Intel
Lead Microprocessors power continues to increase

Courtesy, Intel
Why Scaling?

- Technology shrinks by ~0.7 per generation
- With every generation can integrate 2x more functions on a chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction
Pentium 4

- **Deep pipeline (2001)**
  - Very fast clock
  - 256-1024 KB L2$

- **Characteristics**
  - 180 – 65 nm process
  - 42-125M transistors
  - 1.4-3.4 GHz
  - Up to 160 W
  - 32/64-bit word size
  - 478-pin PGA

- **Units start to become invisible on this scale**
Pentium M

- Pentium III derivative
  - Better power efficiency
  - 1-2 MB L2$
- Characteristics
  - 130 – 90 nm process
  - 140M transistors
  - 0.9-2.3 GHz
  - 6-25 W
  - 32-bit word size
  - 478-pin PGA
- Cache dominates chip area
Core2 Duo

- **Dual core (2006)**
  - 1-2 MB L2$ / core

- **Characteristics**
  - 65-45 nm process
  - 291M transistors
  - 1.6-3+ GHz
  - 65 W
  - 32/64 bit word size
  - 775 pin LGA

- **Much better performance/power efficiency**
Core i7

- **Quad core (& more)**
  - Pentium-style architecture
  - 2 MB L3$ / core
- **Characteristics**
  - 45-32 nm process
  - 731M transistors
  - 2.66-3.33+ GHz
  - Up to 130 W
  - 32/64 bit word size
  - 1366-pin LGA
  - Multithreading
- **On-die memory controller**
Atom

- **Low power CPU for netbooks**
  - Pentium-style architecture
  - 512KB+ L2$

- **Characteristics**
  - 45-32 nm process
  - 47M transistors
  - 0.8-1.8+ GHz
  - 1.4-13 W
  - 32/64-bit word size
  - 441-pin FCBGA

- **Low voltage (0.7 – 1.1 V) operation**
  - Excellent performance/power
A plethora of VLSI CAD problems

Devices, interconnects, circuits, systems, signal, power, analog, digital …..
Design Abstraction Levels
Where are we in the design flow?

Specifications

System-level Design

RTL-level Design

Gate-level Design

Transistor/Circuit Level

Layout

Final Verification

Top-down Design

Electrical & Thermal Properties, Delays, Waveforms, Parasitics Effects, Coupling Noise ...

Bottom-up Verification
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, ...)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function
Why circuit analysis?

Performance verification

• A critical step for evaluating expected performance prior to manufacturing

• Simulation is always cheaper and more efficient than actually making the chip

• True more than ever for today’s high manufacturing costs
Why circuit simulation (cont’d)?

- Design optimization/synthesis
  
  ▼ Need to evaluate circuit performances **many times** in an optimization loop before meeting all the specs
  
  ▼ Can only be practically achieved via simulation (models)
Why models?

- Models are integral parts of system simulation and/or optimization

Abstract Executable Models

Cycle Accurate Models

VHDL/Verilog Models

Interconnect Gate Models

Device Models

Cost

Speed
Assessment of simulators

- Accuracy
- Runtime
- Memory

Robustness/Applicability

- Accuracy
- Runtime
- Memory

- Accuracy
- Memory
- Runtime
Selected Topics

► Classical circuit simulation methods (SPICE)
  ▼ LU factorization, Newton’s method
  ▼ (Modified) nodal formulation (MNA)
  ▼ Nonlinear DC analysis
  ▼ AC analysis
  ▼ Linear/nonlinear transient analyses
  ▼ SPICE device models
Many problems are modeled by some form of coupled (nonlinear) first-order differential equations.

For circuit problems this is usually done using MNA formulation.
Write KCL (Kirchoff’s Current Law) at node 1:

\[ C \frac{d (v_1 - v_3)}{dt} + \frac{(v_1 - v_4)}{R} - f(v_2 - v_1) = 0 \]

If we do this for all N nodes:

\[ F(\vec{x}(t), \vec{x}(t), \vec{u}(t)) = 0 \quad \vec{x}(0) = \vec{X} \]

\[ \vec{x}(t) = \text{N dimensional vector of unknown node voltages} \]

\[ \vec{u}(t) = \text{vector of independent sources} \]

\[ F = \text{nonlinear operator} \]
How can we solve this set of nonlinear differential equations?

\[ F(\ddot{x}(t), \dot{x}(t), \bar{u}(t)) = 0 \quad \bar{x}(0) = \bar{X} \]

- Closed-form formula/hand analysis easily becomes infeasible
- Need to develop computer programs (circuit simulators) to solve for the solution numerically
Selected Topics

► Statistical timing analysis & optimization

Variability

- Process Characterization
- Interconnect Gate Models
- Delay Calculators